Transport Property and Charge Trap Comparison for N-Channel Perylene Diimide Transistors with Different Air-Stability[†]

M. Barra,*,[‡] F. V. Di Girolamo,[‡] F. Chiarella,[‡] M. Salluzzo,[‡] Z. Chen,[§] A. Facchetti,*,[§,||] L. Anderson,[⊥] and A. Cassinese[‡]

CNR-SPIN and Department of Physics Science, University of Naples Federico II, Piazzale Tecchio 80125, Naples, Italy, Polyera Corporation, 8045 Lamon Avenue, Skokie, Illinois 60077, Department of Chemistry, Northwestern University, 2145 Sheridan Road, Evanston Illinois 60208, Electronic Materials Research Lab, School of Engineering and Physical Sciences, James Cook University, Townsville QLD 4811, Australia

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N-type organic field-effect transistors (OFETs), based on two perylene diimide semiconductors (PDI-8 and PDI-8CN_2) exhibiting very different air sensitivities, have been fabricated on Si/SiO_2 substrates. These OFETs have been electrically characterized in vacuum both in the dark and under white-light illumination by dc transfer and output curves, bias stress experiments and variable temperature measurements. In particular, the combination of variable temperature and light illumination experiments is shown to be a powerful tool to clarify the influence of charge trapping on the device operation. Even if, in vacuum, the air-sensitive PDI-8 devices display slightly better performances in terms of field-effect mobility and maximum current values, according to our results, charge transport in PDI-8 films is much more affected by charge trap states compared to PDI8-CN_2 devices. These trapping centers are mainly active above 180 K, and their physical nature can be basically ascribed to the interaction between silanol groups and water molecules absorbed on SiO_2 surface that is more active above the H_2O supercooled transition temperature.

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1. Introduction

Organic field-effect transistors (OFETs) are of interest for the fabrication of low cost, flexible, and large area logic circuitry.[1−4] In OFETs, the electrical transport is an interfacial phenomenon, since the charge motion is confined in a thin region (a few molecular layers) at the interface between the semiconducting and the dielectric layers and the dielectric barrier.[5,6] Hence, the physical and chemical surface properties of the dielectric film can strongly affect the overall device operation.[7,8] For a long time, the search for organic semiconductors displaying efficient electron transport capabilities (n-type compounds) in field-effect devices was unsuccessful. Indeed, compared to holes, electrons have shown far greater sensitivity to trap sites located on the dielectric surface.[9] Furthermore, the number of n-type compounds operating in ambient conditions (air-stable) remains very limited to date. Among the n-type semiconductors for OFETs, perylene carboxylic diimide derivatives are undoubtedly one of the most interesting classes, since they provide high carrier mobility (between 0.1 and 1 $cm^2/(V\ s)$)[10] and can be used in combination with gold electrodes for efficient electron injection. Depending on the molecular structure, perylene diimide-based transistors exhibit very different behavior concerning their air-stability.[11] It was recently demonstrated that the introduction of strong electron-withdrawing substituents (cyano and/or fluoro-alkyl groups) in the perylene molecule core can tune the orbital energetics, which makes electron transport less sensitive to trapping by O_2 and H_2O.[12] For these systems, electron mobilities as high as 0.1−3 $cm^2/(V\ s)$ have been demonstrated for OFETs fabricated and measured in air.[13,14]

In core-cyanated perylenes, the LUMO energetic levels are shifted down by 0.4−0.6 eV in comparison with the unsubtituted systems. However, the influence of the film microstructure and morphology on the air-stability of this class of molecules and the possible presence of a steric barrier limiting the diffusion of electron-trapping environmental gases toward the dielectric interface are also under debate.[15,16] All these recent experimental works have defined a general scientific paradigm, claiming that n-type compounds characterized by good air-stability are less affected by the chemical structure of the dielectric surface.[8] The weak mobility dependence on the dielectric surface chemistry of air-stable n-type semiconductors, such as copper perfluorocyanene and core-cyantated perylene diimides, was ascribed to their low sensitivity to electron trapping mechanisms due to the interaction between charge carriers and interfacial silanol, hydroxyl, and/or carbonyl group functionalities.

In this paper, with the goal to shed light on this fundamental issue, charge transport in bottom-gate bottom-contact transistors based on two perylene diimide compounds with similar morphological and microstructural characteristics,[11,12] but where the corresponding FETs exhibit very different air-stabilities, has been investigated. The two n-type semiconductors employed in this study are *N,N'*-bis(*n*-octyl)-perylene-3,4:9,10-bis(dicarboximide) (PDI-8, air sensitive) and *N,N'*-bis(*n*-octyl)-1,6-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2 or Polyera ActivInk N1200, air insensitive). Both compounds were vapor-deposited on Si (gate)/bare SiO_2 (dielectric)/Au (contacts) substrates for transistor fabrication. The bare SiO_2 surface of the Si/SiO_2 substrates has a large number of Si−OH (silanol) groups, thus a considerable amount of electron-trapping sites.[17] AFM images have been recorded to study the film microstructure. The transistor electrical properties have been assessed in terms of variable-temperature transfer-curves, bias stress experiments, and hysteresis analysis. A special focus has been given to investigate the combined effects of temperature variation and

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* Corresponding author. (M.B.) E-mail: mbarra@na.infn.it. Phone: ++39-0817682548. (A.F.) E-mail: a-facchetti@northwestern.edu.
[‡] University of Naples Federico II.
[§] Polyera Corporation.
[||] Northwestern University.
[⊥] James Cook University.

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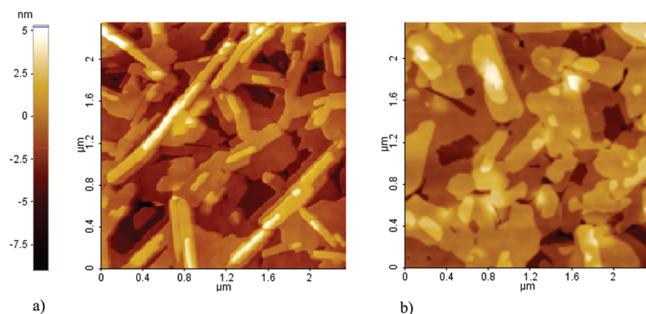

Figure 1. Atomic force microscopy (AFM) images (size 2.4 × 2.4 μm^2) of (a) PDI-8 and (b) PDI-$8CN_2$ thin films.

light illumination on the device electrical response. In vacuum, field-effect mobility values extracted in saturation regime for air-unstable PDI-8 transistors are about 3× higher than those evaluated for PDI-$8CN_2$ FETs. On the other hand, as a result of their sensitivity to SiO_2 surface traps, PDI-8 devices are more influenced by the bias stress effect (BSE) and displayed peculiar behaviors in the temperature range above 180 K both in the dark and under illumination.

2. Results

2.1. Film Deposition and Morphology. PDI-8 and PDI-$8CN_2$ (Polyera ActivInk N1200) powders were purchased from Sigma-Aldrich and Polyera Corporation, respectively. Films were evaporated by Knudsen cells in a high vacuum system (base pressure between 10^{-7} and 10^{-8} mbar) on Si^{++}(500 μm)/SiO_2(200 nm) substrates, provided with gold (bottom-contact) source-drain interdigitated electrodes ($L = 40$ μm, $W = 22$ mm). Before the deposition, the substrates were cleaned, in sequence, in ultrasonic baths of acetone and ethanol, followed by a drying in pure N_2 gas.

The same evaporation conditions were used for the deposition of both perylene films. A deposition rate of 1 nm/min was used while keeping the entire chamber at 100 °C. More details about the deposition method can be found elsewhere.[18] Film thickness was fixed at 30 nm. The surface morphology of the perylene films was analyzed by a XE100 Park AFM microscope in air (true noncontact mode with amplitude regulation) and by an Omicron VT-AFM microscope operating in ultra high vacuum conditions (pressure $<10^{-10}$ mbar, noncontact mode with frequency shift feedback control). Images were acquired using silicon doped cantilevers (resonance frequency around 300 kHz) provided by Nanosensor.

Atomic force microscopy (AFM) images in Figure 1 show the surface morphology of PDI-8 and PDI-$8CN_2$ films. Both films are polycrystalline, with the crystallites organized in a ribbon-like grain structure, in good agreement with previous strudies.[11,12] For both PDI-8 and PDI-$8CN_2$ films, the terrace heights are around 19.5 ± 0.5 Å. This result is consistent with a film microstructure where the semiconductor molecules grow with the long c axis almost perpendicular to the substrate surface and a molecular tilt angle of ~40°. The terrace edges of PDI-8 films are preferentially faceted and more elongated in one preferential direction, while PDI-$8CN_2$ films exhibit more rounded grains. The root-mean-squared-roughness of these films is similar, i.e., 1.7 ± 0.1 nm for PDI-8 and 1.8 ± 0.1 nm for PDI-$8CN_2$. The semiconductor surface is characterized by only 3−4 atomically flat terraces.

2.2. OFET DC Characterization: Output and Transfer Curves. Unless otherwise stated, all electrical tests were performed in vacuum (10^{-4} mbar) and in the dark immediately

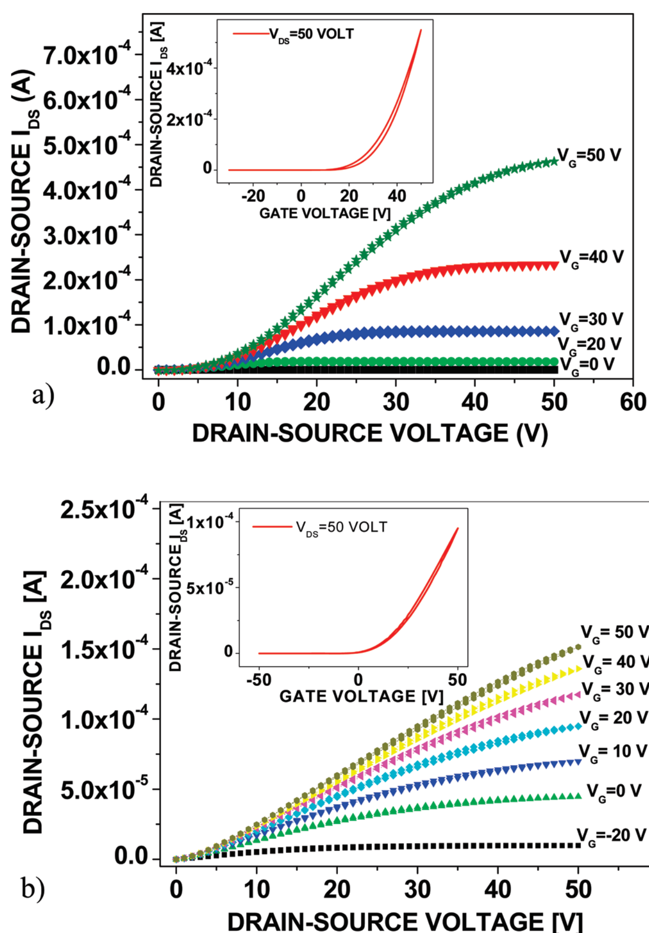

Figure 2. Room temperature output curves of (a) PDI-8 and (b) PDI-$8CN_2$ transistors. In the inset, the corresponding transfer curves in saturation region (V_{DS} = 50 V).

after the transistor fabrication, using a cryogenic probe-station connected to a Keithley 487 picoammeter and a Keithley 2400 voltmeter. The output curves in Figure 2a reveal that the electrical response of the PDI-8 transistors is significantly affected by the contact resistance (R_c) contribution, since for drain-source (V_{DS}) voltages lower than 10 V the I_{DS} current displays a marked sublinear behavior, far from the predictions of the ideal MOSFET model.[19] The charge carrier mobility (μ) of these FETs, evaluated in the saturation region (see the corresponding transfer-curve in the inset of Figure 2a), is ~0.1 $cm^2/(V\ s)$, being one order of magnitude higher than that extracted in linear region. This occurrence is another consequence of the R_c contribution and is in good agreement with other experimental data reported in literature for the same material where $R_c \sim 2-4 \times 10^4$ Ω cm (in saturation) were measured.[20a] For PDI-8 transistors, the onset voltage V_{on}, defined here as the voltage where the device current exceeds the lower limit of the experimental setup (1 nA), is very close to 0 V.

The electrical response of the PDI-$8CN_2$ devices (see Figure 2b) presents quite different features. Here, the contact resistance R_c at low biases is probably lower and the output curves follow the predicted linear behavior at small V_{DS} values. However, comparable R_c value of $\sim 5 \times 10^4$ Ω cm were recently measured in saturation for bottom-gate bottom-contact (Au untreated) FETs.[20b] Thus, for the purpose of the discussion below when analyzing the temperature-dependence FET characteristics in saturation, injection barrier difference between PDI-8 and PDI8-CN_2 does not play a major role. Since the values of the onset voltage V_{on} are largely negative ($V_{on} < -20$ V)[12], the PDI-

$8CN_2$ transistors exhibit non negligible currents (in the range of μA) even when the gate-source voltage (V_{GS}) is zero. Mobility values for PDI-$8CN_2$ (see the inset in Figure 2b for a typical transfer-curve in saturation) are similar in the linear and saturation regions, being about 0.02−0.03 cm^2/(V s), in good agreement with the results reported by Yoo et al. for PDI-$8CN_2$ bottom-contact transistors on bare SiO_2 substrates.[21] The gate voltage dependence of the conductivity (σ) extracted from the data reveals, at $V_{GS} = V_{DS} = 50$ V, that PDI-8 σ is ~4× higher than that of the core-cyanated perylene. This discrepancy is very similar to the value observed for mobility, and consequently, a contribution coming from different densities of induced charge carriers should be excluded. Electrical tests performed in air confirm that the PDI-$8CN_2$ devices are stable in ambient conditions. For this compound, the difference between the mobility values extracted in air and vacuum is in the range of 20−30%. Conversely, PDI-8 FETs are inactive after a few seconds of air exposure, and no detectable I_{DS} current is recorded at any V_{GS} by our experimental setup.

2.3. Bias Stress Effects. After the standard dc characterization, the electrical response of PDI-8 and PDI-$8CN_2$ transistors has been investigated with respect to bias stress effects (BSEs). This phenomenon is usually observed by the shift of the V_{th} threshold voltage with time, due to the prolonged application of gate-source V_{GS} voltages which drive the device in the accumulation region. The same phenomenon can be analyzed by monitoring the I_{DS} time decay upon static voltage polarization (fixed V_{DS} and V_{GS}). The physical origin of the BSE is ascribed to the action of deep trap states related to semiconductor chemical instability, intrinsic structural defects (e.g., grain boundaries), and/or external impurities and/or chemical functionalities present on the dielectric surface.[22] For all fabricated devices, BSE has been investigated by recording the I_{DS} time curves under an applied gate bias V_{GS} of +50 V. The drain-source voltage V_{DS} has been fixed at +5 V for PDI-$8CN_2$ and at +20 V for PDI-8 to reduce the R_c contribution which strongly affects the electrical response of the PDI-8 devices at small V_{DS} values. The experimental curves have been compared with the predictions of the stretched exponential function[23]

$$I = I_0 \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \tag{1}$$

This function accounts for the dispersive nature of the BSE by the two parameters β and τ. Indeed, the trap states responsible for this electrical instability are characterized by a wide energy distribution, located below the conduction band edge for n-type semiconductors and with different characteristic times of the elementary trapping events. The comparison between the experimental stress measurements and the fitting curves obtained from eq 1 for representative PDI-8 and PDI-$8CN_2$ transistors is reported in Figure 3. The resulting values of β and τ are shown in the inset of the same figure.

This analysis reveals that PDI-8 FETs are much more sensitive to BSE than PDI-$8CN_2$ devices. Indeed, for the former the current decreases >40% after 1000 s of V_{GS} application, whereas for the latter the current reduction is limited to ~20%. This difference is well summarized by the τ values which are inversely proportional to the decay rate. For PDI-$8CN_2$, τ is about 5 times higher than for PDI-8. Concerning this comparison, it should be outlined that, according to the literature, BSE dynamics are strongly affected by the accumulated charge (n_s) density in the transistor active channel. In our work, this value is comparable for all bias stress measurements, since, in any

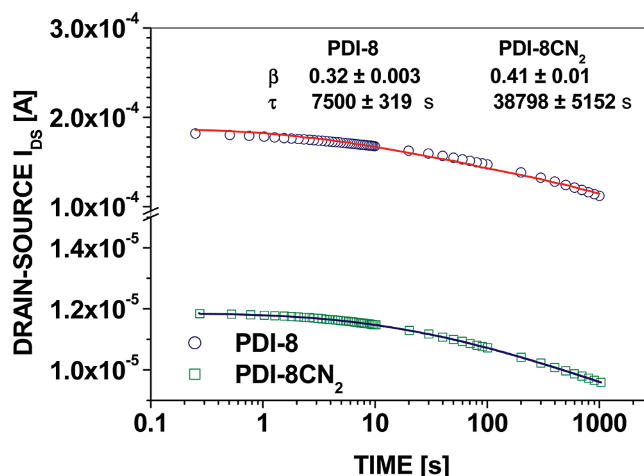

Figure 3. Bias stress curves (symbols) and corresponding fitting curves (solid lines) for PDI-8 and PDI-$8CN_2$ transistors.

case the same $V_{GS} = 50$ V and the same C_{ox} for the dielectric barrier have been utilized. The influence on the BSE parameters of the V_{DS} voltage is usually considered negligible,[22] even if other recent reports claim that the use of higher V_{DS} voltages reduce the BSE occurrence.[24] Given that $V_{DS} = 20$ and 5 V have been used for PDI-8 and PDI-$8CN_2$ devices, respectively, this consideration seems to further support the conclusion that charge transport in the core-cyanated compound is much more robust with respect to the BSE.

2.4. Variable Temperature Measurements in Darkness. Variable temperature measurements are a well-established and powerful tool to investigate physical mechanisms ruling the charge transport in semiconductors. Indeed, they have been widely employed to obtain information about the presence of trap states and their influence on the electrical properties of these materials. For organic field-effect devices, it has been demonstrated that this type of measurement is extremely effective in quantifying trapping effects related to specific chemical groups present on the dielectric surface.[25] Here, to further analyze the differences between the field-effect responses of the two perylene derivatives, the transfer-curves of the PDI-8 and PDI-$8CN_2$ transistors have been recorded, initially in the dark, in the temperature range between 295 and 90 K. For PDI-$8CN_2$ FETs in the dark (Figure 4a), the current decreases when the temperature is reduced, as expected for materials with a thermally activated charge transport.

In this regime, FET charge transport is dominated by thermally activated hopping mechanisms and the extracted mobility (see the inset in Figure 4a) can be modeled in good approximation by an Arrhenius law

$$\mu = \mu_0 e^{-E_a/KT} \tag{2}$$

This type of behavior is theoretically predicted by the so-called multiple trap and release (MTR) model.[26] According to this model, the charge motion can be described as a dynamic sequence of trapping and thermally activated release events, involving shallow energy states localized just below the conduction edge. Equation 2 is derived directly by this model, if the simplifying assumption of the existence of a single discrete trap state level at energy E_T is made. In this case, the activation energy E_a represents the energy difference between the conduction band-edge and E_T. The value of E_a evaluated for the PDI-$8CN_2$ transistors between room temperature and 130 K is ~100

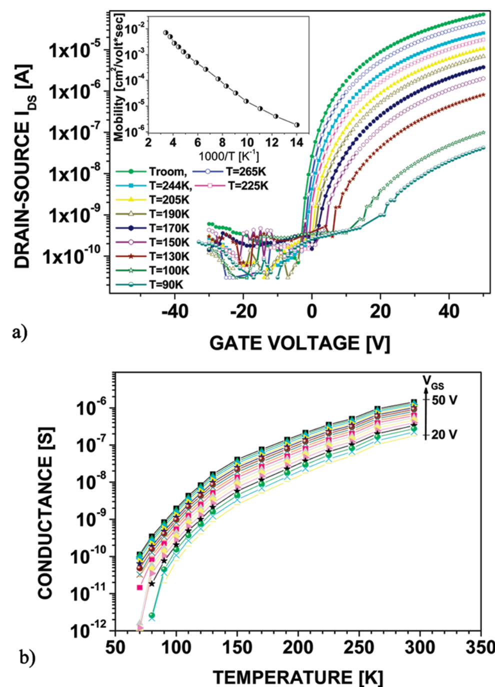

Figure 4. (a) Variable-temperature transfer curves in saturation and (b) conductance curves at different V_{GS} measured in dark for a PDI-8CN_2 transistor. The inset of Figure 4a shows the Arrhenius plots (μ vs $1/T$) of the extracted mobility.

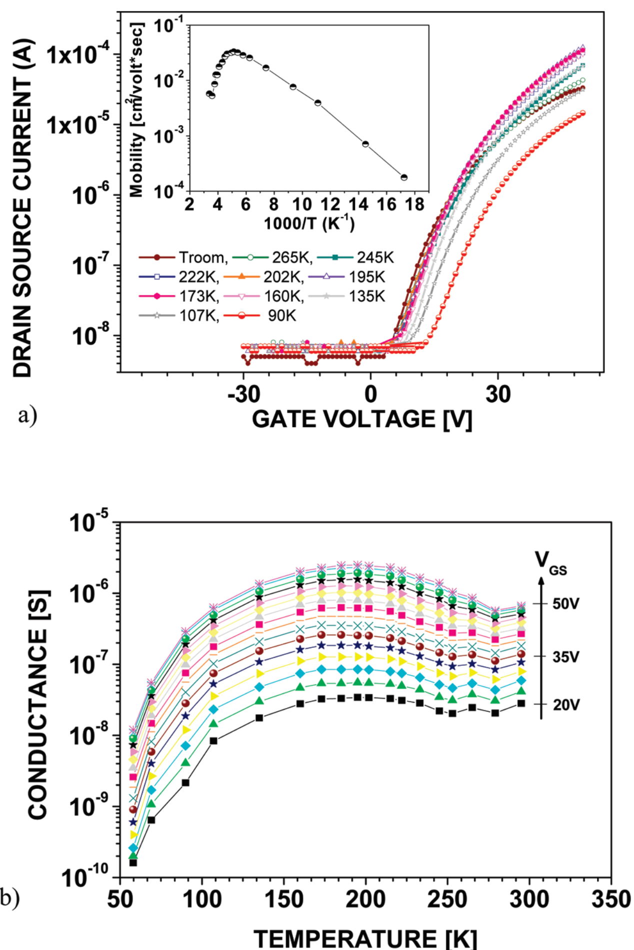

Figure 5. (a) Variable-temperature transfer curves in saturation and (b) conductance curves at different V_{GS} measured in dark for a PDI-8 transistor. Panel a shows the Arrhenius plots (μ vs $1/T$) of the extracted mobility.

meV and decreases at lower temperatures, where temperature-independent tunnelling mechanisms could play a significant role.[27] As shown, the onset voltage V_{on} shifts toward more positive values with decreasing temperature. Indeed, the thermal energy reduction lowers the probability for a charge to be promoted in the conduction states (released by the trapping centers) and implies that, in order to form an accumulation layer suitable for the conduction, the V_{GS} voltage should be increased. For PDI-8CN_2, the thermally activated behavior of mobility is consistently reproduced by the conductance (I_{DS}/V_{DS}) curves at different V_{GS} displayed in Figure 4b.

The variable-temperature transfer curves of the PDI-8 transistors exhibit a peculiar behavior (see Figure 5a). The device current in the transfer-curves increases when the temperature decreases from room temperature (295 K) to about 190 K. The extracted mobility temperature dependence (see the inset in Figure 5a) follows the same trend and has its maximum at about 200 K. The thermally activated behavior of μ, as described by eq 2, becomes predominant only below this temperature, where the value of E_a is ~50 meV. It should be also noted that the onset voltage V_{on} remains almost unchanged up to 200 K and starts to increase only at lower temperatures, in agreement with thermally activated behavior. Conductance curves in Figure 5b clarify that the current behavior in the range between 295 and 190 K tends to be more and more temperature-independent at decreasing gate-source V_{GS} voltages, presenting a well-defined maximum of the conductivity around $T = 200$ K.

2.5. Variable Temperature Measurements under Illumination. The effects of light irradiation on the electrical response of organic transistors have been the subject of recent studies suggesting the possibility of using light as an additional control parameter to extend the device functionalities.[28−30] The most direct consequence of the visible light illumination on the OFET operation is the photogeneration of additional mobile charge carriers, exceeding the equilibrium densities, and the related current enhancement at any gate-source voltage.[28,29] However, light exposure usually magnifies transfer-curve hysteresis, suggesting that under illumination charge transport in OFETs is more sensitive to basic trapping processes.[30] To date, most of the studies concerning the interaction with light have been focused on p-type transistors, while very little attention has been dedicated to investigating the same effects in n-type devices.[31] For comparison with variable temperature measurements performed in the dark, the transfer-curves of the PDI-8 and PDI-8CN_2 transistors have been analyzed as a function of temperature (in the range between 340 and 90 K) under light irradiation. For these measurements, devices were illuminated by a microscope white light lamp (MICRO-LITE FL 3000) through the optical window of the probe-station. The distance between the light source and the device surface was about 3 cm. A circular light spot with a diameter of 1.6 cm was utilized to provide a uniform illumination of the transistor active channels. A preliminary calibration was performed by a photodiode to measure the light power density (P_L), which in our experiments was fixed at about 200 mW/cm^2. Before the beginning of the thermal cycle, transistors were illuminated during a period of 5 min in order to get a steady state condition. Then, transistors were illuminated during the whole thermal cycle with an average duration of about 3 h. This procedure allowed the influence on the transistor electrical response of the long-term electrical memory effects induced by the continuous repetition of light switching to be eliminated.[31] No appreciable degradation of the transistor electrical response as a consequence of the light irradiation was detected in our experiments.

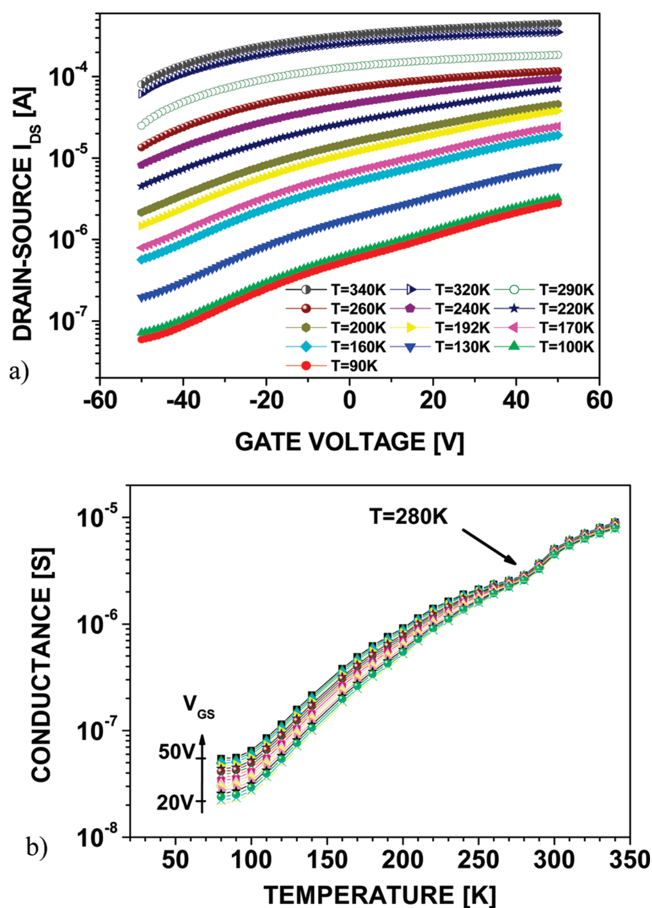

Figure 6. (a) Variable temperature transfer-curves in saturation and (b) related conductance curves at different V_{GS} under light illumination for a PDI-8CN$_2$ transistor.

Figure 6a shows the variable temperature transfer-curves under light illumination for a PDI-8CN$_2$ transistor. These measurements reveal that the OFET response is largely affected by carrier photogeneration and the current exceeds largely the lower limit (1 nA) of the experimental setup at any V_{GS}. The shape of the curves varies with temperature, and at lower ones, where the darkness field-effect mobility is negligible, the I_{DS} current displays an almost exponential dependence on the V_{GS}. The on−off current ratio increases with decreasing temperature, going from ∼5 at $T = 340$ K to ∼40 at $T = 90$ K. Similar to the devices measured in the dark, the current in transfer curves increases with the temperature. The current monotonic behavior is also clear in the conductance curves (Figure 6b), even if a small anomaly in the slope appears in the temperature region around 280 K.

The measurements for the PDI-8 transistors (Figure 7a) demonstrate that light illumination magnifies the unusual $I-V$ behavior observed at different temperatures. The current-temperature dependence is again strongly nonmonotonic and the effect of the light is largely dependent on the temperature. The conductance curves in Figure 7b highlight that, between 300 and 180 K, the charge transport is dominated by effects which cannot be described in the framework of a thermally activated mechanism. Indeed, the current abruptly decreases when the temperature varies from 300 to 280 K and then remains almost constant down to 250 K. Finally, a new very sharp increase is detected going from 250 to 180 K. Below this temperature, the current starts again to decrease at any V_{GS}. For the PDI-8 devices, the light-induced current enhancement at negative V_{GS} voltages (depletion region) is quite limited. Consequently, the ON-OFF ratios are still in the range of

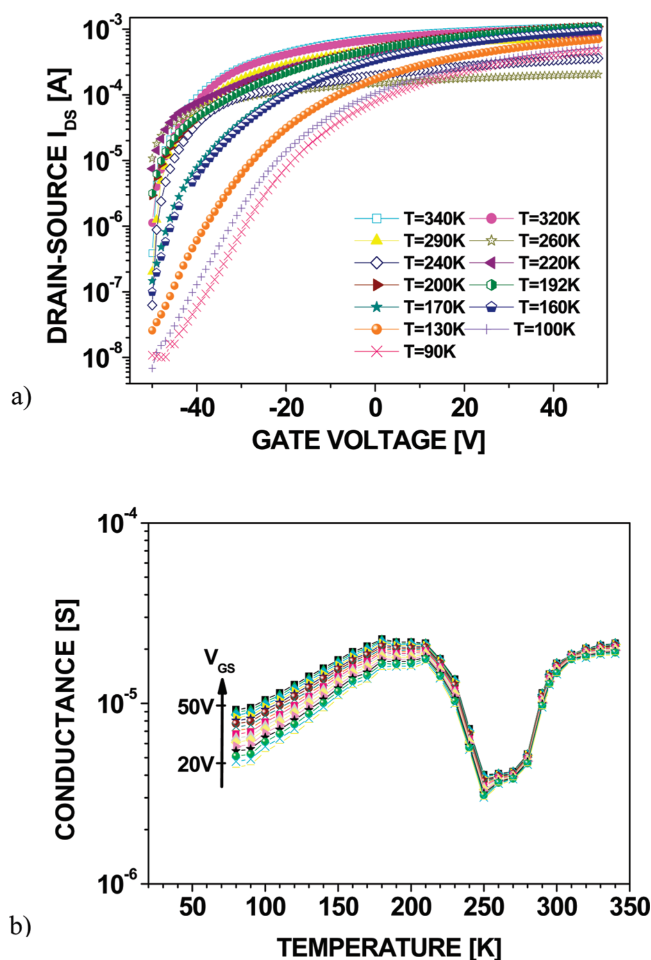

Figure 7. (a) Variable temperature transfer-curves in saturation and (b) related conductance curves at different V_{GS} under light illumination for a PDI-8 transistor.

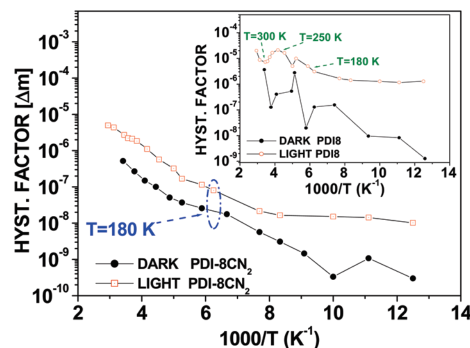

Figure 8. Variable temperature hysteresis factor (Δm) in the dark (closed symbols) and under illumination (open symbols) for a PDI-8CN$_2$ transistor. The inset shows the corresponding curves for a PDI-8 transistor.

10^3-10^4, being reduced in the temperature region where the current anomalies are dominant.

Further insight into the electrical response of the PDI-8CN$_2$ and PDI-8 devices is provided by the temperature dependence of the $I-V$ hysteresis in the transfer-curves. For both in the dark and under illumination measurements, Figure 8 reports the hysteresis factor (Δm), defined as the difference between the slopes of the forward and backward transfer-curves measured at $V_{GS} = 50$ V, as a function of temperature.[32] Similar to previous reports,[30] light magnifies the hysteresis occurrence. For both perylene compounds, the temperature dependence of the hysteresis factor is quite different in the temperature regions

above and below 180 K. For all devices, below this temperature value Δm is strongly reduced and only slightly temperature dependent. Above 180 K, the hysteresis behavior of two perylene compounds is very different. The peculiar temperature dependence of the mobility and conductance of PDI-8 devices is reproduced also in the hysteresis data, which show the maximum values in the temperature range where the conductance is reduced. Conversely, for PDI-8CN$_2$ Δm is thermally activated above 180 K with an activation energy close to 100 meV. This occurrence demonstrates the sensitivity of the hysteresis data, in comparison with mobility and conductance measurements, to reveal the influence of trapping sites even on the charge transport of PDI-8CN$_2$ devices.

3. Discussion

The experimental data reported in this work show the different electrical responses of PDI-8 and PDI-8CN$_2$ transistors realized on Si/SiO$_2$ substrates. The maximum saturation mobility and current values measured for PDI-8 FETs are always higher by ~3−4 times than those of PDI-8CN$_2$ transistors. Even if no significant morphological difference between the two perylene films has been detected by AFM, this occurrence can be tentatively ascribed to the slightly lower intermolecular distance in PDI-8 vs PDI8-CN$_2$ molecules. Although the crystal structure of PDI-8 in unknown, that of several PDIR (R = alkyl) derivatives are known[33] and are characterized by similar brick-like packing characteristics and typical intermolecular distances of ~3.2−3.3 Å vs similar packing but slightly larger core−core distance of 3.43 A for PDI-8CN$_2$ due to the presence of the cyano groups.[34]

The output plot analysis at low drain voltages (linear regime) reveals that PDI-8CN$_2$ contact resistance is somewhat lower than that of PDI-8 devices although saturation contact resistance were measured to be in the same range (vide supra). Given the difference between the LUMO energy (E_{LUMO}) values for the two perylene compounds,[11] this occurrence may be the results of the higher energy barrier for electron injection from Au electrodes in the case of PDI-8. The reasons for the different values of the onset voltage V_{on}, which in the dark is close to 0 V for PDI-8 and largely negative (<-20 V) for PDI-8CN$_2$, may also be the result of the larger electron affinity of the cyanated derivative, resulting in unintentional doping.

Concerning the bias stress effects, as shown by Miyadera et al.,[23] charge trapping by chemical functionalities at the interface with the dielectric is much more relevant than charge traps induced by microstructural disorder (grain boundaries). Our results seem to support this conclusion. Indeed, PDI-8 and PDI-8CN$_2$ films have similar microstructures, morphologies and surface roughness. Therefore the relevant differences in the BSE can be attributed entirely to the trapping at the interface. Consequently, the increased sensitivity of PDI-8 on BSE phenomenon is a first demonstration of its weakness with respect to the action of dielectric surface traps.

Variable temperature measurements performed in the dark and under illumination showed that, while the charge transport in the PDI-8CN$_2$ transistors is basically ruled by classical thermally activated mechanisms, the electrical properties of the PDI-8 devices is dominated by extrinsic effects, mainly operating at temperatures between 300 and 180 K. Gomez et al.[35] highlighted the occurrence of electrical instabilities in the response of many different types of polycrystalline and amorphous organic thin-film transistors in the temperature region around 200 K. This experimental evidence was ascribed to the confinement of residual water molecules in the organic layers, playing a prominent role in trapping processes involved in BSE and displaying a supercooling behavior very close to 200 K. The presence of water molecules absorbed on the SiO$_2$ interface was also claimed to be the physical origin for the generation of a discrete trap state during the operation of Pentacene single crystal field-effect devices.[25] In this case, the basic charge trapping phenomena were found to be different above and below 280 K. These results suggest that the anomalies observed in the electrical response of the PDI-8 devices are related to the same type of water traps.

On bare SiO$_2$ substrates, the underling mechanism for the formation of trapping and/or scattering of charge carriers is the strong chemical interaction between absorbed H$_2$O molecules and silanol (−SiOH).[8] The water molecules confined at the dielectric interface show complex changes in density exactly in the range between 300 and 180 K.[36] This result points out a strict correlation between the trapping effectiveness and the thermal expansion dynamics of water molecules. Since similar SiO$_2$ substrates and growth conditions (chamber temperature and evaporation rate) were considered for both PDI-8CN$_2$ and PDI-8 films, the peculiar temperature behavior of the latter devices can be attributed to the higher sensitivity of PDI-8 on the above-described trapping mechanisms operating on the dielectric surface. Finally, it is also important to outline that the action of the above-discussed charge trapping processes could be further enhanced in the regions near the source-drain electrodes, in presence of an increased structural disorder in the growth of the organic layer.[37] This possibility cannot be excluded at this stage and is worth of future investigations by means of multiprobe electrical measurements, able to selectively analyze the conducting properties of different regions of the transistor active channels.

4. Conclusions

Various types of dc characterizations (i.e., variable-temperature transfer curves, bias stress experiments, and hysteresis analysis) have been performed in this work to investigate the general paradigm that air-stable n-type organic semiconductors are less sensitive to the surface chemistry of the dielectric layer used for field-effect device fabrication. In analyzing the charge transport of two perylene n-channel semiconductors grown on unfunctionalized Si/SiO$_2$ substrates, the contribution of energy states related to the confinement of water molecules in the bulk of the film and at the dielectric interface has to be accurately taken into account. According to the results of this study, these electron trap states are active in vacuum only above $T = 180$ K. Furthermore, given the similarity of the morphological features of the two perylene films here analyzed, these states are not directly related to the semiconductor film microstructure. Our results confirm that the n-type compounds with lower lying LUMO levels (PDI-8CN$_2$) are less sensitive to this type of traps and, at the same time, they are air-stable. The tuning of the orbital energetics, with the introduction of strong electron withdrawing substituents, is therefore a general and effective approach to design organic compounds with more robust electron transport characteristics.

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