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Induction Motor Drives Fed by an NPC Inverter with Unbalanced DC-Link

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Abstract: Neutral Point Clamped (NPC) converters with n levels are traditionally controlled in such a way that the DC-link capacitors operate at $1/(n-1)$ of the total DC-link voltage level. The voltage level across the DC-link capacitors has to be properly regulated by the capacitor unbalance control to contain the harmonic distortion of the converter output voltages. State-of-the-art modulation techniques address the problem of the DC-link voltage regulation for NPC inverters. However, they highly show reduced performance when unbalanced DC-link voltages are considered. In this paper, a novel Space Vector Modulation (SVM) is proposed for NPC converters with an unbalanced DC-link. At every modulation interval, the technique defines the optimal switching pattern by considering the actual unbalanced DC-link conditions. The proposed modulation allows improving the harmonic content of the NPC converter output voltage with respect to a traditional ML-SVM, when the same operating conditions are considered. As an extension, the proposed modulation technique will guarantee the same output voltage quality of a traditional ML-SVM with unbalanced DC-link, while improving the conversion efficiency thanks to a reduction of switching frequency.

Keywords: Neutral Point Clamped (NPC); SVM; inverter; unbalanced DC-links; modulation technique

1. Introduction

The widespread adoption of Voltage Source Inverters (VSIs) has pushed research forward in the development of new power converter topologies and modulation techniques, which take into account the non-linear behavior of power semiconductors and components with the aim of improving the performance of the whole power conversion system [1–3]. In medium- and high-power applications, Neutral Point Clamped (NPC) inverters [4] are prevailing over conventional two-level VSIs, thanks to their high performance, such as reduced stress on semiconductors, less switching losses, lower Electromagnetic Interference (EMI), and improved harmonic content thanks to the n levels of the output voltage waveform. A NPC inverter with n levels takes its name from the typical structure of the DC-link bus, composed by $n-1$ capacitors forming several Neutral Points (NPs). To maximize the performance of this architecture, the voltages of the $n-1$ capacitors must be controlled to be equal to $1/(n-1)$ of the total DC-link voltage.

The main issue for this kind of power converter is the low-frequency oscillation of the NPs' voltage due to current paths that can involve them. The balancing of NPs voltages is usually achieved by adjusting the application duration of the redundant vectors when Space Vector Modulation (SVM) or carrier-based PWM (CBPWM) with the zero-sequence component injection are adopted [5–11]. However, these modulation techniques do not completely allow to overcome the problem of the

voltage fluctuation of the NPs as described in [12]. In fact, some output voltage space vectors introduce an unbalanced between the capacitors' voltages that cannot be compensated using the vectors redundancies, especially for high modulation indexes and low power factors, [5]. Therefore, low harmonic content of the output voltages can be guaranteed with a traditional multilevel SVM (ML-SVM) [13] or CBPWM if the capacitors' voltages are balanced and have a low ripple. This is usually achieved increasing the switching frequency causing higher losses, especially in high power density applications with small DC-link capacitors, [2]. NPC topology is also gaining attention in some application fields characterized by the need of independently regulating several DC-link voltages. In photovoltaic (PV) generation systems, the Maximum Power Point Tracking (MPPT) algorithm can be independently implemented on series-connected PV strings with related DC-link capacitors with the aim of increasing the power extractions from the PV panels [14,15]. In these cases, the unbalanced DC-link reduces the performance of traditional SVM for NPC converter.

To address the distorted output voltage and current due to unbalanced DC-link, several modulation techniques have been developed for 3 levels (3L)-NPC converter based on CBPWM with appropriate zero-sequence component injection or modified SVM [16–19]. The SVM presented in [16] is based on a complex space vector diagram causing time-consuming calculation of the duty cycles. The approach of zero-sequence presents some complications for the generalization and the implementation of the modulation strategy [17]. New and interesting approaches are proposed in [18,19] aiming at implementing a fast-processing method to calculate the duty cycles on the basis of virtual output voltage space vectors.

The authors propose an analytic approach for the development of a novel SVM that has the aim to reduce the harmonic content of the output voltage of a 3L-NPC converter for a given unbalanced DC-link condition. The proposed SVM considers the time-variant voltage unbalance across the DC-link capacitors during the modulation period in order to calculate the duty cycles of the real output voltage space vector [20]. In detail, starting from a mathematical model of the 3L-NPC inverter with unbalanced DC-link, the proposed model-base solution allows calculating the vectors duration independently from the load parameters.

In this paper, performance analysis of the proposed modulation technique is presented for a 3L-NPC inverter feeding an induction motor. Section 2 reports the mathematical model of the NPC when an unbalanced DC-link is considered. Section 3 describes the proposed modulation technique, while Sections 4 and 5 analyzes the validity of the proposed techniques through numerical and experimental results when compared to traditional SVM.

2. Model of the NPC Inverter with Unbalanced DC-Link

Figure 1 shows the electric circuit of a three-phase 3L-NPC inverter. The space vector of the inverter output voltage **v** is:

$$\mathbf{v} = \frac{2}{3}\left\{v_{ao} + v_{bo}\exp\left(j\frac{2\pi}{3}\right) + v_{co}\exp\left(j\frac{4\pi}{3}\right)\right\} \tag{1}$$

where j represents the unit imaginary number, v_{xo} is the output voltage of the generic x-th leg with $x \in \{a, b, c\}$. Table 1 reports v_{xo} for the three possible switching states of the x-th leg defined by means of the state variable δ_x. S_{ix}, with $i \in \{1, 2, 3, 4\}$, are Boolean quantities representing the state of the power switches of the x-th leg. For 3L-NPC inverter with unbalanced DC-link, the voltages across the capacitors are function of the voltage unbalance (ΔV) between the capacitors as follows:

$$v_{C_1} = +\frac{V_{dc}}{2} - \Delta V \qquad v_{C_2} = +\frac{V_{dc}}{2} + \Delta V \tag{2}$$

Thus, the output voltage of the x-th leg can be expressed combining Table 1 and Equation (2):

$$v_{xo} = \delta_x\frac{V_{dc}}{2} - |\delta_x|\Delta V \qquad \text{with } x \in \{a, b, c\} \tag{3}$$

The expression of the space vector of the output voltage in unbalanced condition can be written by subsisting Equation (3) into Equation (1) as:

$$\mathbf{v} = \frac{V_{dc}}{3}\left\{\delta_a + \delta_b \exp\left(j\frac{2\pi}{3}\right) + \delta_c \exp\left(j\frac{4\pi}{3}\right)\right\} - \frac{2}{3}\Delta V\left\{|\delta_a| + |\delta_b| \exp\left(j\frac{2\pi}{3}\right) + |\delta_c| \exp\left(j\frac{4\pi}{3}\right)\right\} \quad (4)$$

For a generic switching pattern k, defined by the set $\{\delta_a, \delta_b, \delta_c\}$, the space vector $\mathbf{v}_k$ of the inverter output voltages can be expressed as follows:

$$\mathbf{v}_k = \mathbf{v}_k^* + \frac{2}{3}\gamma_k \Delta V_k \quad (5)$$

where $\mathbf{v}_k^*$ represents the voltage space vector corresponding to balanced DC-link, while ΔV_k is the unbalanced voltage corresponding to the switching pattern k, and where γ_k is given by:

$$\gamma_k = -\left\{|\delta_a| + |\delta_b| \exp\left(j\frac{2\pi}{3}\right) + |\delta_c| \exp\left(j\frac{4\pi}{3}\right)\right\} \quad (6)$$

Figure 2 shows the 19 output voltage space vectors of the 3L-NPC inverter in case of balanced DC-link [20]. They can be classified on the basis of their magnitude in zero $|\mathbf{v}_0| = 0$, small $|\mathbf{v}_{Sn}| = \frac{1}{3}V_{dc}$, medium $|\mathbf{v}_{Mn}| = \frac{1}{\sqrt{3}}V_{dc}$ and large vectors $|\mathbf{v}_{Ln}| = \frac{2}{3}V_{dc}$, with $n \in \{1, 2 \ldots 6\}$. The small vectors can be achieved using two different switching patterns. This redundancy are used to control the DC-link capacitor voltages. The unbalance DC-link condition affects just the small and medium vectors. With reference to the unbalanced condition of the Figure 3 ($\Delta V = -\frac{1}{6}V_{dc}$), medium vectors change their magnitude and phases because γ_k is perpendicular to $\mathbf{v}_k$. These variations determine the displacement of the vectors along the perimeter of the $\frac{2}{3}V_{dc}$ hexagon towards one of the two adjacent large vectors depending on the sign of the voltage unbalance ΔV, as shown by the green vectors of Figure 3. Small vectors change only their magnitude because γ_k has the same direction of $\mathbf{v}_k$. Therefore, the small vectors lose the redundancy in unbalanced DC-link condition becoming twelve distinct vectors, which are depicted in orange and blue in Figure 3.
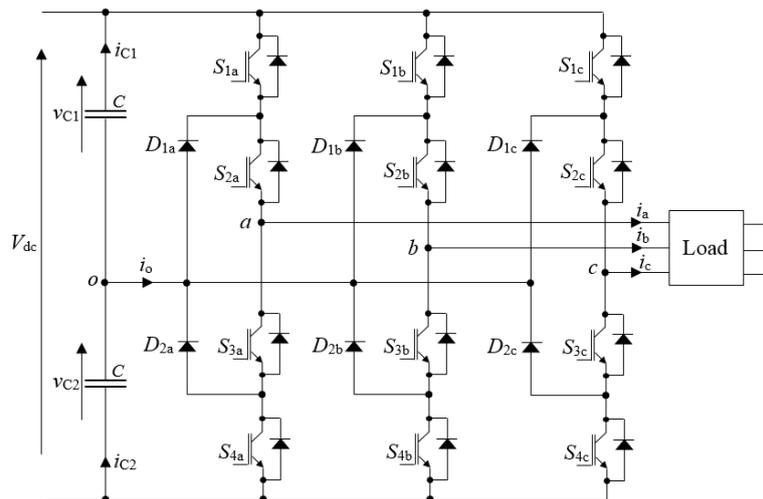

Figure 1. Scheme of the 3L-NPC converter.

Table 1. Switching states and output voltages v_{xo} with $x \in \{a, b, c\}$.

S_{1x}	S_{2x}	S_{3x}	S_{4x}	Switching State δ_x	Output Voltage v_{xo}
1	1	0	0	1	$+v_{C_1}$
0	1	1	0	0	0
0	0	1	1	-1	$-v_{C_2}$

The neutral point current i_o can be calculated by the following equation:

$$i_o = -\left(|\delta_a|i_a + |\delta_b|i_b + |\delta_c|i_c\right) = \gamma_k \cdot \mathbf{i} \tag{7}$$

where $\mathbf{i}$ is the space vector of the inverter output current defined by:

$$\mathbf{i} = \frac{2}{3}\left\{i_a + i_b \exp\left(j\frac{2\pi}{3}\right) + i_c \exp\left(j\frac{4\pi}{3}\right)\right\} \tag{8}$$

It is always true that:

$$v_{C_1} + v_{C_2} = V_{dc} \quad \Longrightarrow \quad \frac{dv_{C_1}}{dt} + \frac{dv_{C_2}}{dt} = 0 \tag{9}$$

thus, the following relation can be yield:

$$i_o = -i_{C_1} + i_{C_2} = C\left(\frac{dv_{C_1}}{dt} - \frac{dv_{C_2}}{dt}\right) = 2C\frac{dv_{C_1}}{dt} = -2C\frac{d(\Delta V)}{dt} \tag{10}$$

By considering the Equation (7), the following equation can be obtained:

$$\frac{d(\Delta V_k)}{dt} = -\frac{1}{2C}\gamma_k \cdot \mathbf{i} \tag{11}$$

Therefore, the integration of Equation (10) allows determining the ΔV evolution during the switching pattern k as it will be shown in the following section.
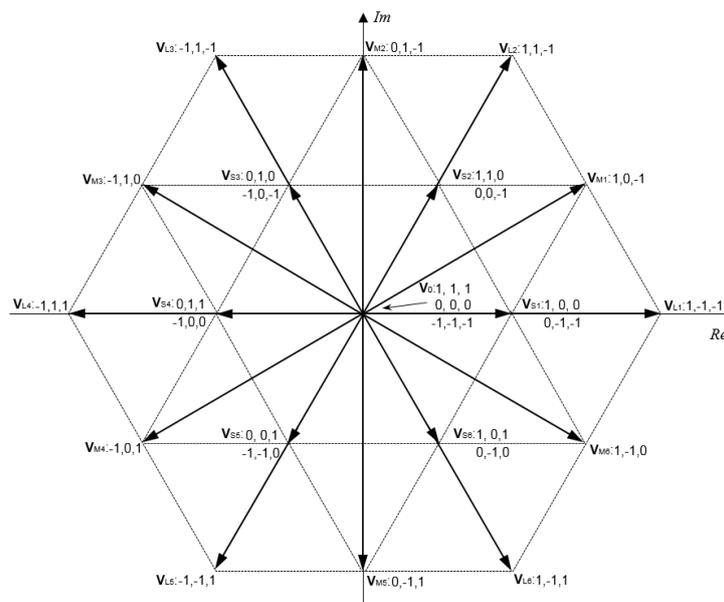

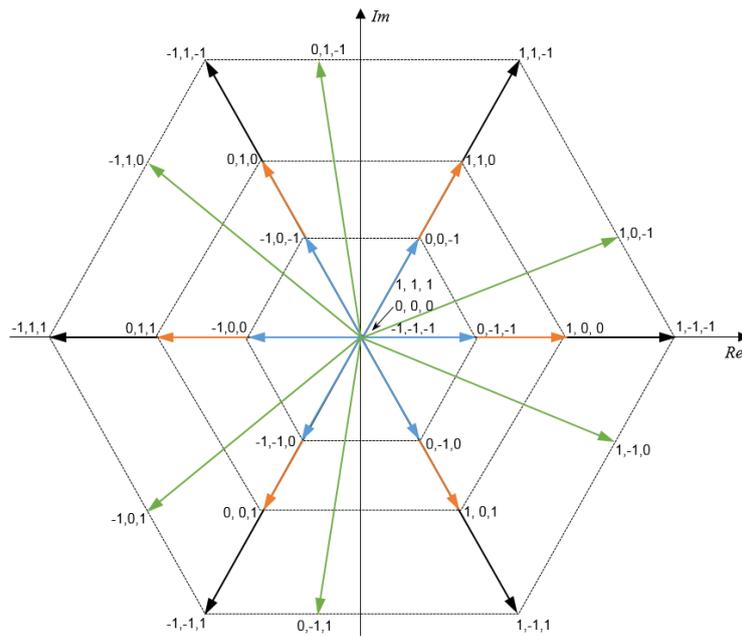**Figure 2.** Voltage space vectors in case of balanced DC-link.

Figure 3. Voltage space vectors in case of unbalanced DC-link ($\Delta V = -V_{dc}/6$).

3. SVM with Unbalanced DC-Link

Traditional SVM for 3L-NPC inverter is based on the hexagon of Figure 2 [13]. If voltage unbalance occurs between the DC-link capacitors, traditional SVM cannot guarantee that, within each modulation period, the space vector of the inverter output voltage matches the reference one. Furthermore, the waveforms of the output voltages have an increased harmonic content.

In this paper, this issue is addressed by means of a novel SVM technique that considers the "true" displacement of the voltage space vectors in unbalanced DC-link condition. Thus, it does not consider only the voltage unbalance at the beginning of the modulation period ($\Delta V(0)$), but the whole time evolution of $\Delta V(t)$ as function of the switching pattern k.

In order to evaluate the function $\Delta V_k(t)$, corresponding to the voltage space vector $\mathbf{v}_k$, a *RL* symmetric load is assumed. Under this hypothesis, the inverter output current space vector $\mathbf{i}_k$ can be calculated as following:

$$\mathbf{i}_k(t) = \left[\mathbf{i}_k(0) + \frac{1}{L}\int_0^t \left(\mathbf{v}_k^* + \frac{2}{3}\,\gamma_k\,\Delta V_k(t)\right) \cdot \exp\left(\frac{R}{L}t\right) dt\right] \exp\left(-\frac{R}{L}t\right) \tag{12}$$

Since $\mathbf{v}_k^*$ is constant during the modulation interval k, Equation (12) yields the following:

$$\mathbf{i}_k(t) = \mathbf{i}_k(0)\exp\left(-\frac{R}{L}t\right) + \frac{\mathbf{v}_k^*}{R}\left[1 - \exp\left(-\frac{R}{L}t\right)\right] + \frac{2}{3L}\exp\left(-\frac{R}{L}t\right)\gamma_k\int_0^t \Delta V_k(t)\exp\left(\frac{R}{L}t\right) dt \tag{13}$$

By substituting the current space vector expression into Equation (10), the following equation can be obtained:

$$\frac{d(\Delta V_k)}{dt} = -\frac{1}{2C}\gamma_k \cdot \left\{\mathbf{i}_k(0)\exp\left(-\frac{R}{L}t\right) + \frac{\mathbf{v}_k^*}{R}\left[1 - \exp\left(-\frac{R}{L}t\right)\right] + \right.$$

$$\left. + \frac{2}{3L}\exp\left(-\frac{R}{L}t\right)\gamma_k\int_0^t \Delta V_k(t)\exp\left(\frac{R}{L}t\right) dt\right\} \tag{14}$$

The derivation of the Equation (14) leads to the following second-order differential equation:

$$\frac{d^2(\Delta V_k)}{dt^2} = -\frac{1}{2C}\,\gamma_k \cdot \left[\frac{1}{L}\exp\left(-\frac{R}{L}t\right)(\mathbf{v}_k^* - R\mathbf{i}_k(0))\right] +$$

$$+\frac{1}{3L^2C}R\exp\left(-\frac{R}{L}t\right)|\gamma_k|^2\int_0^t \Delta V_k(t)\exp\left(\frac{R}{L}t\right)dt - \frac{1}{3LC}|\gamma_k|^2\Delta V_k \quad (15)$$

By imposing the equivalence of integral terms of the Equations (14) and (15), it yields:

$$\frac{d^2(\Delta V_k)}{dt^2} + \frac{R}{L}\frac{d(\Delta V_k)}{dt} + \frac{|\gamma_k|^2}{3LC}\Delta V_k = -\frac{1}{2LC}\,\gamma_k \cdot \mathbf{v}_k^* \quad (16)$$

The differential Equation (16) can be solved by defining the analytical expression of the function $\Delta V_k(t)$ within the time interval in which the voltage space vector $\mathbf{v}_k^*$ is applied. Considering that for a medium and small vector $|\gamma_k| = 1$, while for a large vector $|\gamma_k| = 0$; the following relations can be yield:

$$\begin{cases} \Delta V_k(t) = W_{k,1}\exp(\lambda_1 t) + W_{k,2}\exp(\lambda_2 t) - \frac{3}{2}\,\gamma_k \cdot \mathbf{v}_k^* & \text{if } |\gamma_k| \neq 0 \\ \Delta V_k(t) = \Delta V_k(0) & \text{if } |\gamma_k| = 0 \end{cases} \quad (17)$$

where

$$\lambda_{1,2} = \frac{R}{2L}\left(-1 \pm \sqrt{1 - 4\frac{L}{3R^2C}}\right) \quad (18)$$

$$W_{k,1} = \frac{\dfrac{1}{2C}\,\gamma_k \cdot \mathbf{i}_k(0) - \dfrac{3}{2}\lambda_2\,\gamma_k \cdot \mathbf{v}_k^* - \lambda_2\,\Delta V_k(0)}{\lambda_1 - \lambda_2}$$

$$W_{k,2} = \frac{-\dfrac{1}{2C}\,\gamma_k \cdot \mathbf{i}_k(0) + \dfrac{3}{2}\lambda_1\,\gamma_k \cdot \mathbf{v}_k^* + \lambda_1\Delta V_k(0)}{\lambda_1 - \lambda_2} \quad (19)$$

If $\mathbf{v}^{(r)}$ is the reference voltage space vector to be achieved during the modulation period T_s by means of the SVM switching pattern k, h, i, it yields:

$$\mathbf{v}^{(r)} = \alpha_k\mathbf{v}_k^* + \alpha_h\mathbf{v}_h^* + \alpha_i\mathbf{v}_i^* + \frac{2}{3T_s}\left[\gamma_k\int_0^{\alpha_k T_s}\Delta V_k(t)\,dt + \gamma_h\int_0^{\alpha_h T_s}\Delta V_h(t)dt + \gamma_i\int_0^{\alpha_i T_s}\Delta V_i(t)dt\right] \quad (20)$$

where the functions $\Delta V_k(t), \Delta V_h(t), \Delta V_i(t)$ are evaluated by means of (17)–(19). In detail, the voltage unbalance is calculated by Equation (17) considering the value of $|\gamma_k|$ for every switching pattern. To calculate the coefficients of Equations (18) and (19), the initial voltage and current conditions of every switching patter are imposed equal to the final values achieved at the end of the application of the previous switching patter. Once $\Delta V_k(t), \Delta V_h(t), \Delta V_i(t)$ function have been determined, $\alpha_k, \alpha_h, \alpha_i$ can be calculated by means of the Equation (20) and by imposing

$$\alpha_k + \alpha_h + \alpha_i = 1 \quad (21)$$

Equation (20) is a transcendental equation, and therefore its solution has to be found numerically by means of a root-find algorithm which could require high computational power, limiting the real world implementation of the proposed methodology. Approximating the exponential terms by the first-degree Maclaurin's polynomials, the following closed-form can be used to calculate the values of $\alpha_k, \alpha_h, \alpha_i$:

$$\mathbf{v}^{(r)} = \alpha_k\left[\mathbf{v}_k^* + \frac{2}{3}\gamma_k\Delta V_k(0)\right] + \alpha_h\left[\mathbf{v}_h^* + \frac{2}{3}\gamma_h\Delta V_k(0)\right] + \alpha_i\left[\mathbf{v}_i^* + \frac{2}{3}\gamma_i\Delta V_k(0)\right] \quad (22)$$

where $\Delta V_k(0)$ represents the only needed initial condition, which is the measured voltage unbalance at the beginning of the first switching patter of the modulation period. It has to be underlined that the proposed closed-form solution is independent of the load parameters. Thus, in this paper it is proposed the application of this modulation technique to an electrical drive, in which the 3L-NPC feeds an induction motor controlled by the traditional open-loop *V/f* technique [21]. This choice is justified by the need of properly assessing the performance of the proposed and traditional modulation technique without the impact of the closed-loop control. As example, a Field Oriented Control (FOC) with traditional ML-SVM is controlling a 3L-NPC inverter feeding an induction machine. Due to the unbalanced DC-link voltages, the desired output voltage of the FOC cannot be respected by the SVM causing a torque/speed deviation. At the next sampling interval the the FOC's PI controllers will try to compensate the torque/speed error by defining a new reference voltage affected by the SVM error. Thus the reference voltage defined by the FOC will be affected by the performance of the modualtion technique and the parameters of the PI controllers. This effect will limit the capability of the authors to properly compare the performance of different modulation technique, thus a *V/f* control is selected.

4. Numerical Results

To validate the proposed SVM technique, a numerical model of the three-phase 3L-NPC converter feeding a 1.1-kW induction motor has been developed in MATLAB-Simulink environment. The parameters of the electrical drive are shown in Table 2. The *V/f* motor control and the modulation technique have been modeled using a S-function to facilitate the experimental implementation on a DSP-based control unit. The sampling time and control delays of the experimental setup (Section 5) have been considered for the numerical implementation with the aim of achieving an accurate comparison between numerical and experimental results.

The capacitor unbalanced control is based on a hysteresis algorithm that selects the proper redundant vector [2] at every modulation interval T_s in order of keeping the capacitors' voltages within an desired ΔV. The proposed modulation technique based on Equation (22) is simulated considering a balanced capacitors' voltages reference $v^*_{C_1} = v^*_{C_2} = 200$ V. ΔV, the switching frequency f_{sw}, and load torque T_1 are respectively set to $5\% \cdot V_{dc}$, 2 kHz, and 3.5 Nm. The performance of proposed SVM are compared with the ones of a traditional SVM proposed in [13] in terms of current Total Harmonic Distortion THD_i with the same unbalanced DC-link conditions, for different values of the modulation index ($m = \sqrt{3}|\hat{\mathbf{v}}|^{(r)}/V_{dc}$, where $|\hat{\mathbf{v}}|^{(r)}$ represents the peak value of the reference voltage space vector). Figures 4 and 5 respectively show the motor currents for the traditional SVM and the proposed one when a low value of the modulation index is requested by the motor feeding algorithm ($m = 0.27$). In Figure 6, it is possible to notice how the DC-link capacitors' voltage references are tracked by means of the DC-link balance control for both the modulation techniques. Under the same unbalanced DC-link condition, the traditional SVM cannot accurately synthesize the reference voltage space vector due to the unbalanced DC-link operation at the beginning and during every modulation period. Instead, the proposed SVM allows taking into account the unbalanced voltages by means of Equation (22), independently of the load condition. This leads to a considerable improvement in the quality of the motor currents. The proposed SVM strategy allows reducing THD_i with respect to the traditional modulation by 41.7% in the considered conditions. The performance improvement is also confirmed for a higher value of modulation index ($m = 0.94$). Current waveforms of the traditional and the proposed modulations are respectively depicted in Figures 7 and 8. In this case, the reduction of the THD_i value is equal to 34.7%, when the same voltage ripple across the DC-link capacitors is imposed for the traditional and the proposed SVM as shown in the Figure 9. The reduction of THD_i for different values of the modulation index is reported in Figure 10. The proposed SVM allows improving the performance within the whole interval of the modulation index variation.

Table 2. Parameters of the electrical drive.

1.1-kW Induction Motor		
Rated power	1.1	kW
Rated torque	7.48	Nm
Rated voltage (rms)	380	V
Rated current (rms)	2.65	A
Pole pairs	2	
Stator resistance	7.5	mΩ
Rotor resistance referred to stator	4.8	mΩ
Stator leakage inductance	20	mH
Rotor leakage indutance	20	mH
Air gap inductance	430	mH
Three-Level NPC Inverter		
DC-link voltage, V_{dc}	400	V
modulation period, T_s	500	μs
DC-link capacitor, C	330	μF
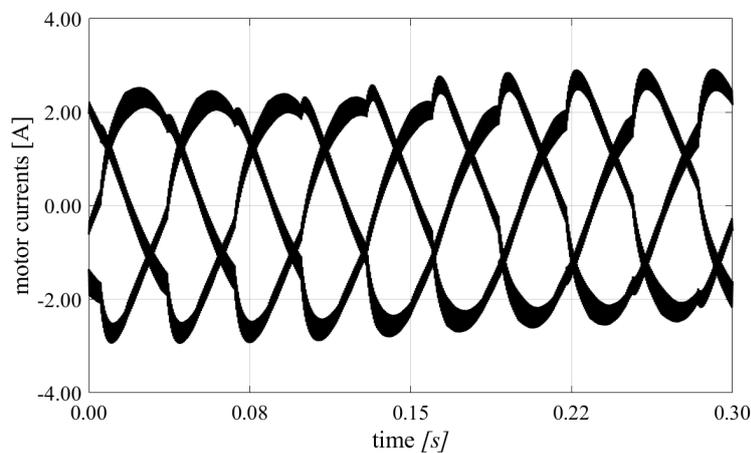
Figure 4. Numerical result: motor currents achieved with the traditional SVM, when $m = 0.27$, $v_{C1}^* = v_{C2}^* = 200$ V, and $T_l = 3.5$ Nm.
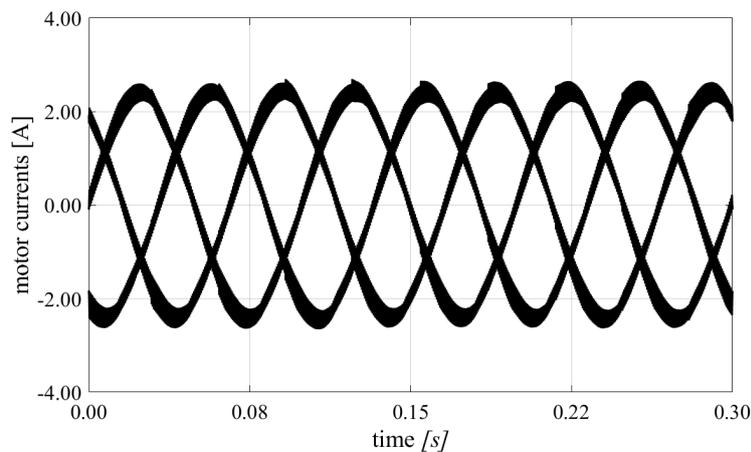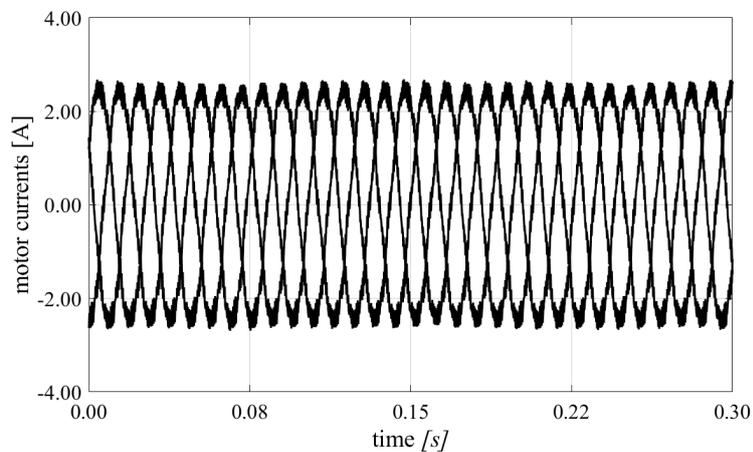

Figure 5. Numerical result: motor currents achieved with the proposed SVM based on Equation (22), when $m = 0.27$, $v_{C1}^* = v_{C2}^* = 200$ V, and $T_l = 3.5$ Nm.
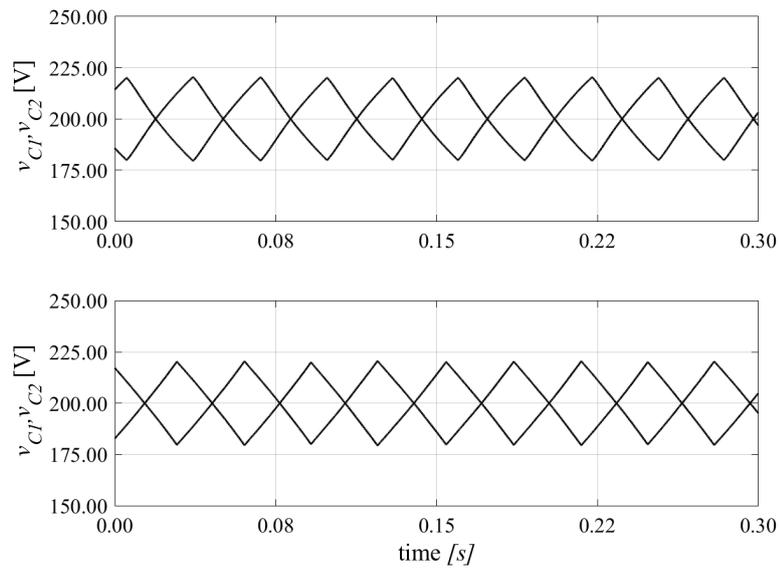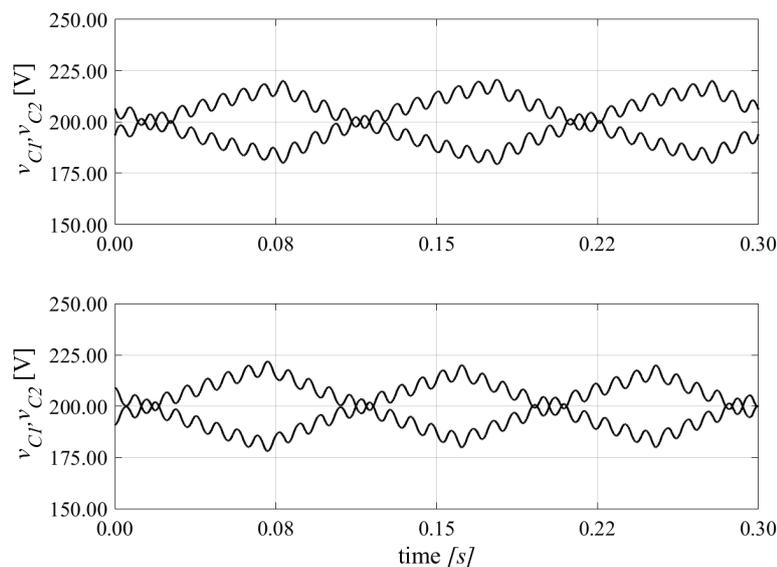
Figure 6. Numerical result: capacitors voltages for the traditional SVM (upper trace) and proposed one (lower trace), when $m = 0.27$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_l = 3.5$ Nm.
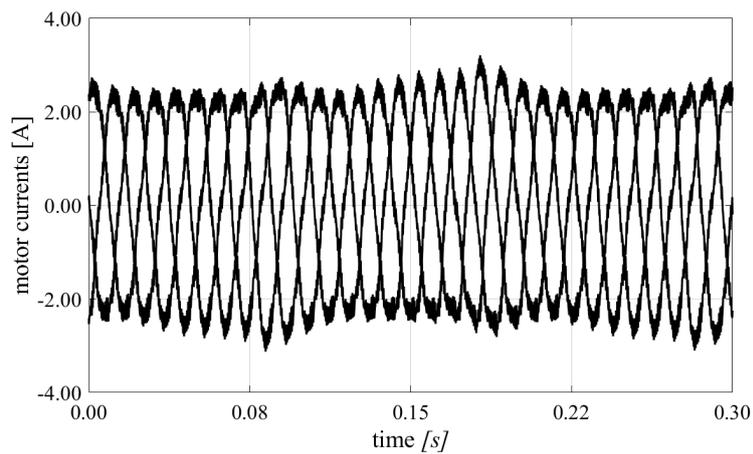

Figure 7. Numerical result: motor currents achieved with the traditional SVM, when $m = 0.94$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_l = 3.5$ Nm.

Figure 8. Numerical result: motor currents achieved with the proposed SVM based on Equation (22), when $m = 0.94$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_l = 3.5$ Nm.

Figure 9. Numerical result: capacitors voltages for the traditional SVM (upper trace) and proposed one (lower trace), when $m = 0.94$, $v_{C1}^* = v_{C2}^* = 200$ V, and $T_1 = 3.5$ Nm.
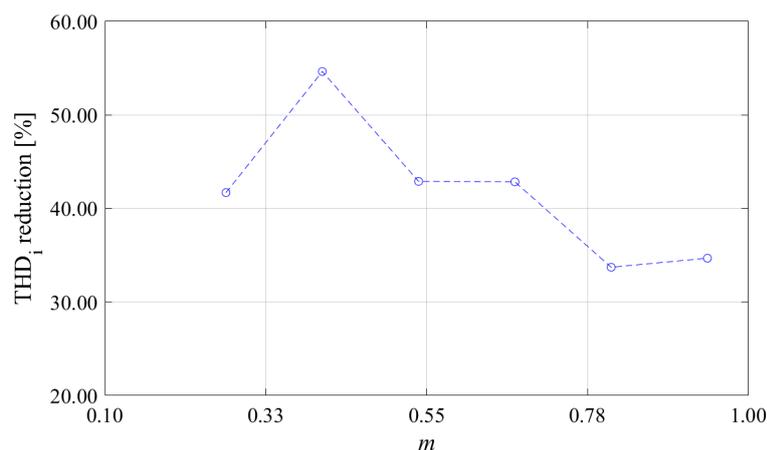
Figure 10. Reduction of the THD_i achieved by means of the proposed modulation technique with respect to the traditional for different values of the modulation index, m.

5. Experimental Results

A full-scale prototype of the 3L-NPC power converter has been designed and manufactured. Every leg of the converter is composed by IGBT module SEMIKRON® SK50MLI066. A picture of the power converter is shown in Figure 11. The experimental control unit consists of DS1006 processor board of a dSPACE® modular system and of an ALTERA FPGA Cyclone III. DS4003 digital I/O board interfaces the two units, which are synchronized by means of an interrupt signal generated by the FPGA board. The synchronizing signal has a period T_s of 500 μs. In detail, the processor unit performs the motor control algorithm and works out the duration and the modulation patterns at every modulation period, which must be imposed in the next T_s, according with the Equation (22) or with traditional SVM [13]. Starting from them, the FPGA unit generates the switching signals with proper dead-time, set equal to 4 μs. The DS2004 board is used to acquire the analog signals from DC-link voltage sensors. The test bench is completed by a 1.1-kW induction motor coupled to a dynamic controllable brake. The main parameters of the test bench are shown in Table 2. To compare the experimental and numerical results, the same tests proposed in Section 4 have been performed. Figure 12 shows the motor currents achieved with the traditional SVM considering the same voltage

references of DC-link capacitors ($v^*_{C_1} = v^*_{C_2} = 200$ V), $m = 0.27$ and the constant load torque $T_1 = 3.5$ Nm. Results achieved with the proposed modulation technique are shown in Figure 13. The improvement in terms of THD_i is comparable with the one achieved in the numerical analysis. The proposed SVM allows achieving a THD_i reduction of 39.2%. In detail, the THD_i decreases from to 11.3%, traditional SVM, up to 6.86% for the proposed solution. Figure 14 shows the capacitor voltage during the test. The experimental results for $m = 0.94$ are reported in Figures 15–17. As it is possible to notice, the proposed modulation technique considerably improves the motor current quality for high values of the modulation index as well. In detail, a reduction of the THD_i equal to 27.7% is achieved with the proposed solution.
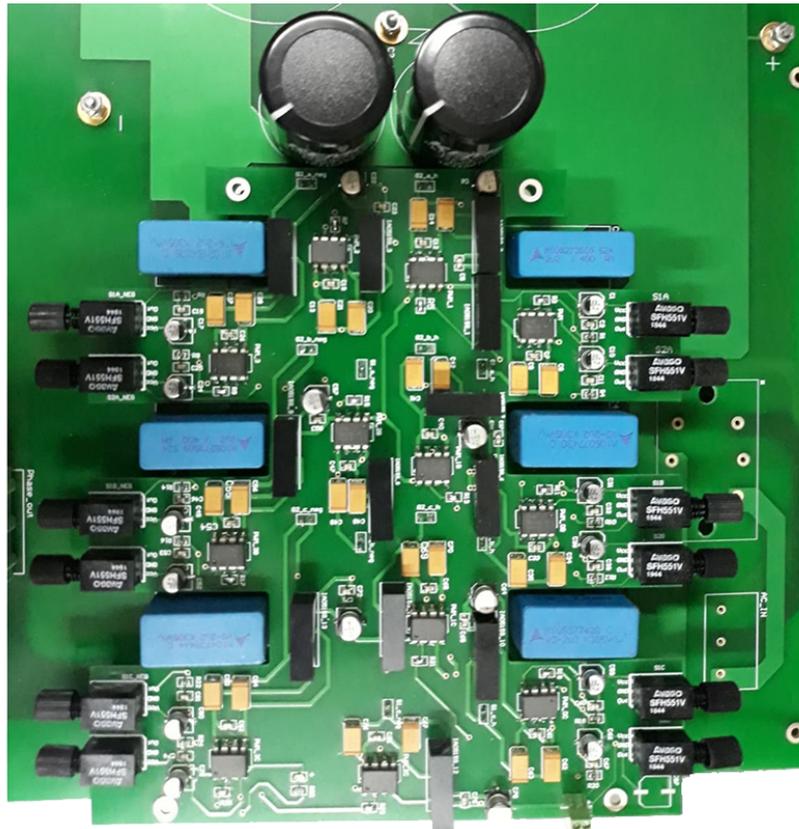
Figure 11. Picture of the three-level NPC inverter prototype.
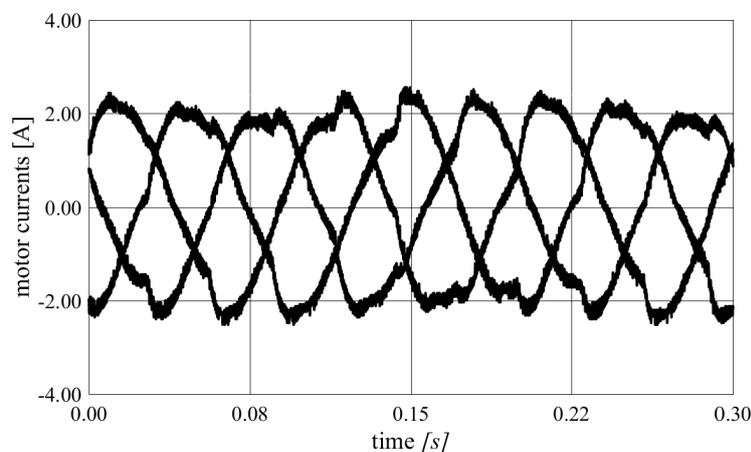

Figure 12. Experimental result: motor currents achieved with the traditional SVM, when $m = 0.27$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_1 = 3.5$ Nm.
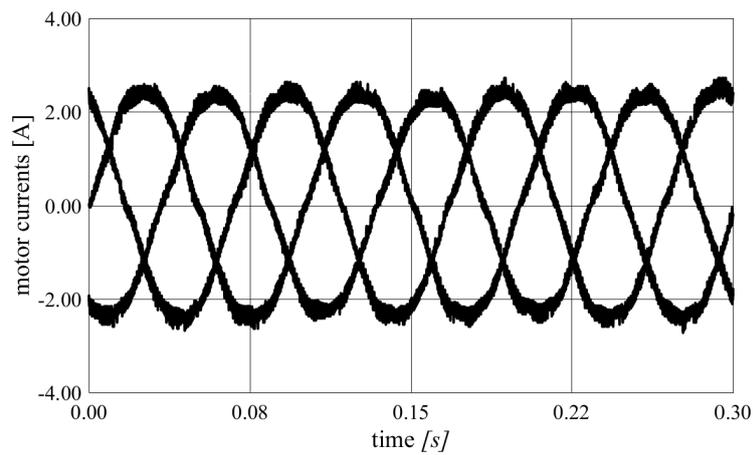
Figure 13. Experimental result: motor currents achieved with the proposed SVM based on Equation (22), when $m = 0.27$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_1 = 3.5$ Nm.
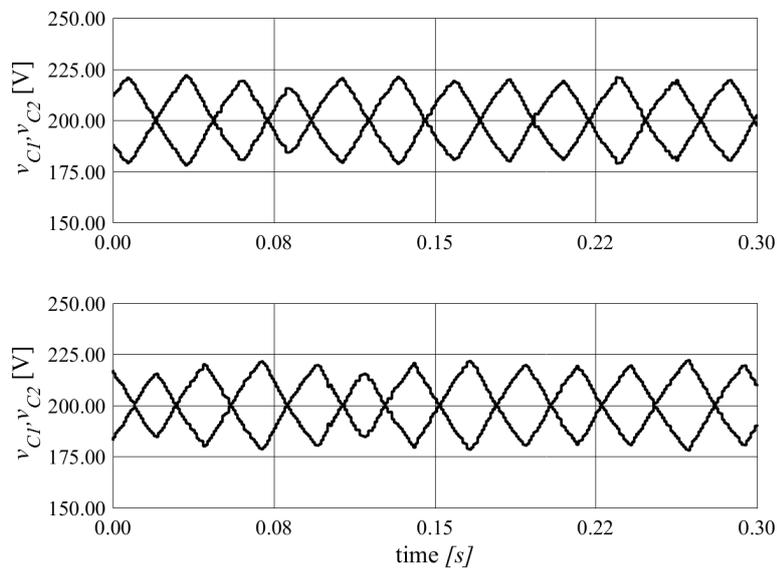

Figure 14. Experimental result: capacitors voltages for the traditional SVM (upper trace) and proposed one (lower trace), when $m = 0.27$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_1 = 3.5$ Nm.
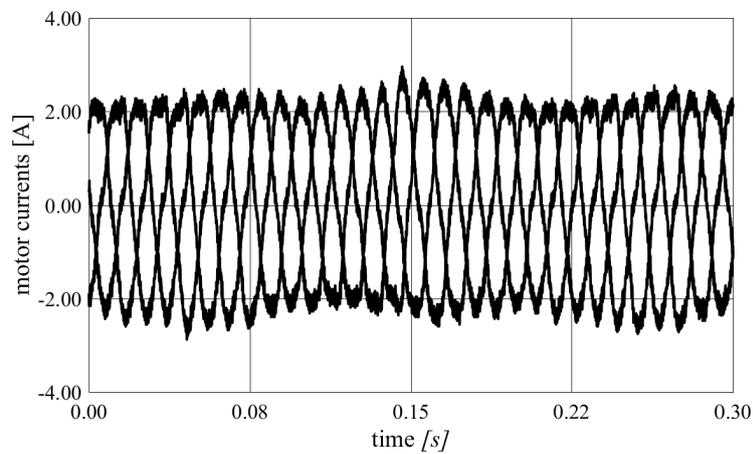

Figure 15. Experimental result: motor currents achieved with the traditional SVM, when $m = 0.94$, $v^*_{C1} = v^*_{C2} = 200$ V, and $T_1 = 3.5$ Nm.
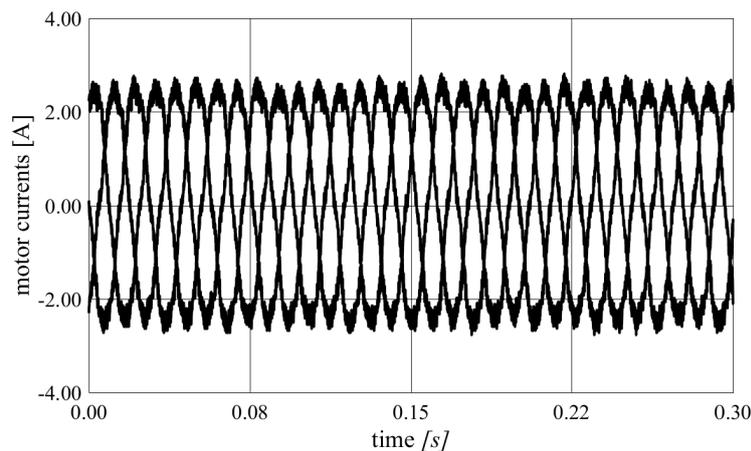
Figure 16. Experimental result: motor currents achieved with the proposed SVM based on Equation (22), when $m = 0.94$, $v_{C1}^* = v_{C2}^* = 200$ V, and $T_1 = 3.5$ Nm.
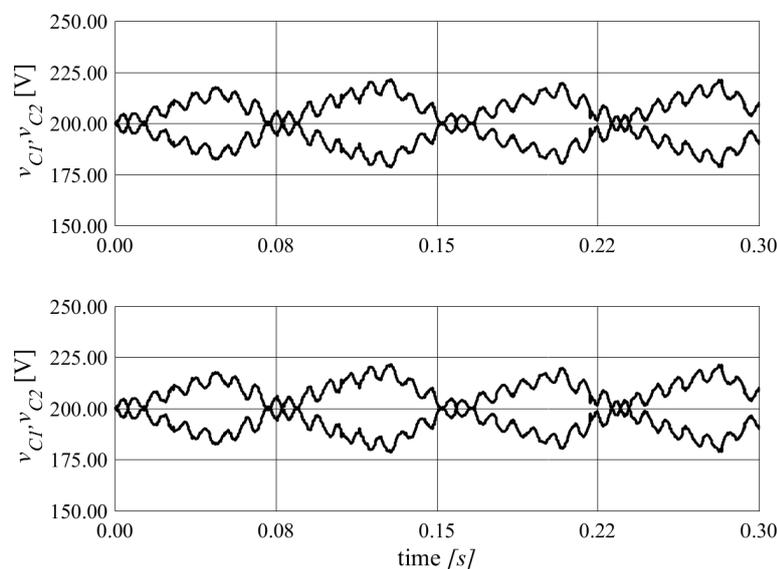

Figure 17. Experimental result: capacitors voltages for the traditional SVM (upper trace) and proposed one (lower trace), when $m = 0.94$, $v_{C1}^* = v_{C2}^* = 200$ V, and $T_1 = 3.5$ Nm.

6. Conclusions

In this paper, a new SVM modulation strategy for a 3L-NPC inverter feeding an induction motor is proposed. It allows improving performances of motor control in terms of reduction of the currents THD thanks to a correct evaluation of the real voltage evolution across DC-link capacitors during unbalanced conditions. The proposed modulation technique does not depend from the specific load parameters and it has a compact and simple formulation structure. This last feature allows achieving low computational cost in the practical implementation. Numerical and experimental results confirm the validity of the proposed SVM strategy in different operating conditions.

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