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# Enhanced fast digital integrator for magnetic measurements

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An enhanced Fast Digital Integrator (eFDI) was prototyped to satisfy the new requirements arising from current on-field exploitation of the previous Fast Digital Integrator in magnetic measurements for particle accelerators at CERN. In particular, the prototype achieves improved performance in terms of offset (5 ppm on 10 V fullscale), self-calibration accuracy (1 ppm of residual error), and data throughput (100 MB/s), by simultaneously preserving high-level signal-to-noise and distortion ratio (SINAD 105 dB at 10 Hz). In this paper, initially, the specifications, the design solutions, and the main features of the eFDI are illustrated. Then, the experimental results of the metrological characterization are compared with the CERN state-of-the-art integrator FDI performance in order to highlight the achieved improvements. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4996539]

## I. INTRODUCTION

Digital integrators[1] are exploited in several measurement principles for disparate measurands, like energy,[2] magnetic field,[3] electrical impedance,[4] and so on.[5] In recent years, research is evolved according to twofold main trends for improving *algorithms*,[1,2,6–11] computing the integral after signal digitization, and *instruments*,[12–22] and carrying out the measurement as a whole. A significant application share is devoted to magnetic measurements and, namely, to *fusion energy* and *particle acceleration*.

In *fusion energy*, integrators have been specifically conceived for measurements on pulsed magnets (septum magnets, bumps, and so on). At Max Planck Institute fur Plasmaphisik, for long-pulse experiments of stellarator Wendelstein 7-X, a lock-in amplifying digital integrator with reduced drift, shortening data processing time by a Field Programmable Gate Array (FPGA), is utilized.[17] Again for long-pulse magnetic fusion devices, an FPGA configured as a digital chopper-integrator for a data acquisition system with 96 channels simultaneously acquiring data at 500 kSa/s per channel, was prototyped.[18]

In *particle acceleration*, a voltage signal is integrated in order to compute the magnetic flux of a magnet, according to Faraday's law.[23] This principle is used in several measurement methods, such as rotating[24–26] and fixed coils, stretched wires,[27] and so on, complemented also by other different techniques (e.g., Hall plates).[28,29] Local and integrated field strength, field direction, harmonics and axis for both low- and high-field conditions are measured.[30] For the final tuning of the superconducting magnets bending the particle beam trajectories of the Large Hadron Collider at the European Organization for Nuclear Research (CERN), an accurate measurement of the field quality was necessary to suitably control the trajectories as well as to focus the beam.[30] Initially, requirements arising from the new generation of fast magnetic transducers[31,32] were not met by the Portable Digital Integrator[33] (PDI) because the accuracy of its voltage-to-frequency converter gets worse at increasing the sampling rate.[30] Several new integrators were conceived at the Commisariat de Energie Atomique (CEA) Saclay,[34] at the Japan Atomic Energy Research Institute,[35] and at the Fermi National Accelerator Laboratory.[36] At BINP,[15] a relative accuracy better than 50 ppm with field duration ranging from 5 $\mu$s was provided. A fully on-board instrument, the Fast Digital Integrator (FDI), exploiting state-of-the-art digitization was developed at CERN, in cooperation with the University of Sannio:[12] Table I shows the main FDI specifications.

FDI was licensed to Metrolab and is exploited as FDI 2056[37] on the field in several application areas:[30] (i) rotating coils for superconducting magnet testing, (ii) vertical cryostat bench, (iii) resistive magnet testing for linear accelerators (Linac4),[38] (iv) magnetic properties bench,[6] and (v) superconducting cable test.[39]

However, experience of on-field applications pointed out the weaknesses and the need for improvement of the current instrument. In particular, mainly self-calibration drawbacks for residual gain and offset errors, e.g., for drift-free long measurements, and a low throughput,[12] e.g., for real-time measurements on pulsed magnets, were pointed out.

In this paper, the enhanced Fast Digital Integrator (eFDI), designed to overcome the above drawbacks of self-calibration and low throughput, is illustrated. In the following, in Sec. II, the eFDI design concept and the specific solutions are shown. In Sec. III, experimental results of eFDI performance characterization in comparison with FDI and PDI are presented.

## II. CONCEPTUAL DESIGN

In this section, (i) the *requirements*, (ii) the *working principle*, (iii) the *basic ideas*, (iv) the *architecture*, and (v) the main improved sections (*analog signal front-end,*

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TABLE I. FDI specifications (UTC: Universal time counter, DNL: Differential Non-Linearity).[12]

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC resolution | | 18 | | | bits |
| Analog input differential | ±5 on each input | | ±10 | | V |
| range (FS) | ±10 on each input | | ±20 | | V |
| ADC sample rate $f_{ADC}$ | 8 programmable values | | | 500 | kS/s |
| External trigger $f_t$ | $f_{ADC} \geq 2f_t$ | | | 250 | kHz |
| Gain | 13 programmable values | 0.1 | | 100 | |
| DC | FS = ±10 V, ±2 $\sigma$ | | | | |
| Digit. DNL | | | 1.5 | | LSB |
| Integ. INL | 30 min, 27 C –36 C | | ±7 ppm | | |
| Integ. stability | 24 h, 30 C | | ±3 ppm | | |
| Integ. repeat. | 30 min, 30 C | | ±1 ppm | | |
| Gain error | 30 min, 27 C –36 C | | 0.2% | | |
| | 24 h, 30 C | | ±0.2% | | |
| Offset error | 30 min, 27 C –36 C | | 17 ppm | | |
| | 24 h, 30 C | | 7 ppm | | |
| AC | $f_{ADC}$ = 500 kS/s, OSR = 100, $f_{in}$ = 1 Hz | | | | |
| Digit. SINAD | | | 97 | | dB |
| Digit. SNHR | | | 103 | | dB |
| Digit. THD | | | –99 | | dB |
| Integ. SINAD | | | 108 | | dB |
| Integ. SNHR | | | 118 | | dB |
| Integ. THD | | | –109 | | dB |
| UTC resolution | | | 50 | | ns |
| Throughput rate | CPCI/PXI bus | | 1 | | MB/s |

*self calibration*, and *digital bus interface*) of the e-FDI are illustrated.

### A. Requirements

In synthesis, the design requirements of eFDI are (i) lower noise level, namely, SINAD of 100 dB in digitizer mode and 120 dB as an integrator, (ii) better input matching for sensing coil signals, on the input impedance values of open, 50 Ω and 1 MΩ, for gain values ranging from 0.01 to 100 in logarithmic scale, (iii) improved self-calibration accuracy (1 ppm of residual error), (iv) higher data throughput of 100 MB/s, and (v) the same metrological challenges of the previous FDI: accuracy requirement of 10 ppm, for at least 1 s of integration time with a bandwidth of 100 kHz.

### B. Working principle

The eFDI has the same working principle of FDI[12] (Fig. 1). The output voltage of a sensor (e.g., a rotating or fixed coil) is digitized [Fig. 1(a)[12]] and integrated over the time interval between two consecutive trigger events. In particular, an integral sample (e.g., a magnetic flux increment) is computed by summing the voltage samples ($V_{k1}, \ldots, V_{ki}, \ldots, V^*_k$) of the Analog-to-Digital Converter (ADC) between the trigger events $\phi_{k-1}$ and $\phi_k$ [Fig. 1(b)]. A loss in measurement accuracy arises from the residual times at the two left and right side ends of the integration time interval [Fig. 1(c)[12]]: (i) $\tau_a$, between the $(k-1)$th trigger pulse $\phi_{k-1}$ and the successive voltage sample $V_1$ and (ii) $\tau_b$, between the *k-th* trigger pulse $\phi_k$ and the previous sample $V*_k$. This inaccuracy is reduced by means of interpolation. At this aim, the trigger event is recognized by a time base [Fig. 1(c)[12]]. This working mechanism is carried out by eFDI *on line*, namely, an integration result is released on the PXI bus at each trigger sample.

### C. Basic ideas

The conceptual design of the e-FDI was based on the following main basic ideas:

- *DAC-based self-calibration*: the twofold drawbacks of static correction, (i) accuracy, arising from the lack of ALU in FPGA, and (ii) thermal drift, deriving from the voltage reference provided by a resistor network, are overcome by a fully digital solution mainly based on a 20-bits DAC with an Integral Non-Linearity (INL) of 1 ppm (1-bit);[40]
- *DMA- and master-based bus controller*: data throughput transfer on the bus PXI (PCI eXtensions for instrumentation[41]) is increased by replacing the compact PCI I/O accelerator PLX 9030,[42] with 33 MHz clock and burst transfers up to 100 MB/s, with the PLX 9056[43] with 66 MHz clock, capable of direct memory access (DMA) and bus mastership;
- *higher-gain lower-noise programmable gain amplifier*: main design concern is to face the enhancement challenges without loosing in metrological dynamic performance; therefore, an analog front end as well as a new optimized printed circuit board (PCB) routing are conceived. The analog front end is mainly composed by

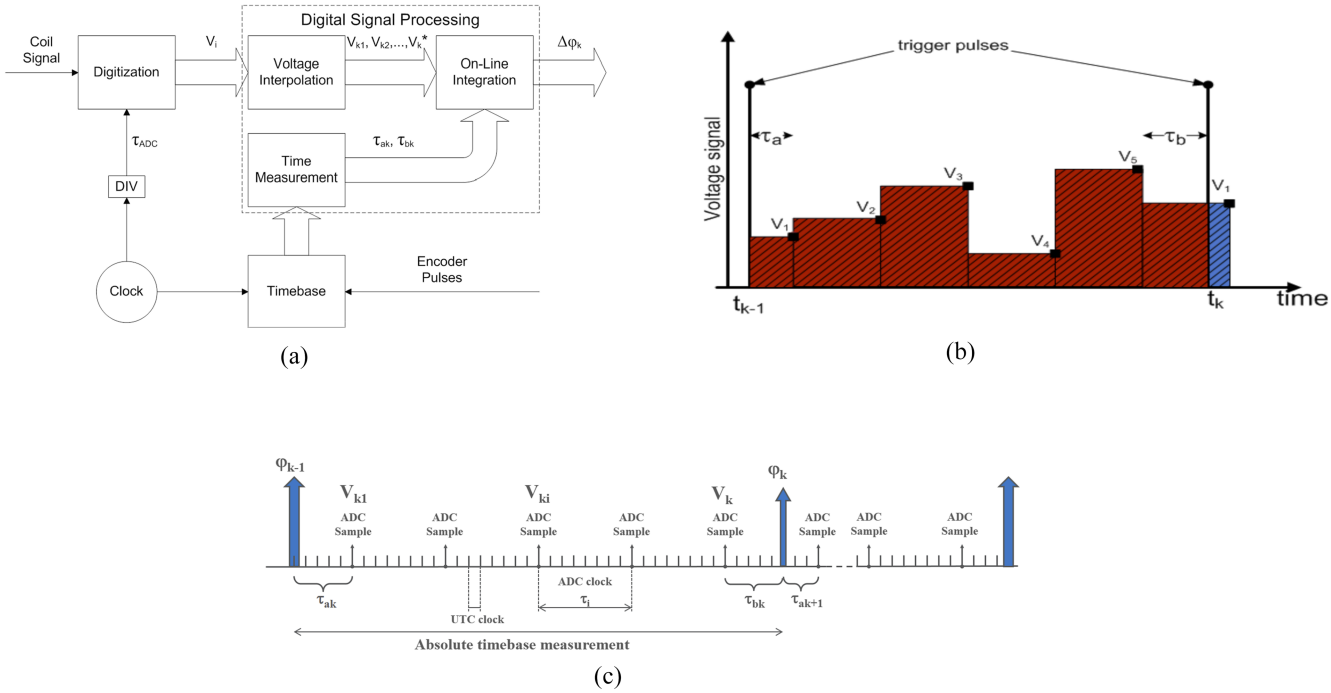


FIG. 1. eFDI working principle: (a) concept architecture,[12] (b) integration, and (c) fine interpolation.[12]

(i) a new anti-alias filter for best matching the sensor output to the digitization chain, based on an optimized input stage with selectable impedance adjustment, (ii) a high-common-mode rejection ratio (CMRR), low-offset, low noise, and distortion analog programmable amplifier based on AD8599,[44] and (iii) a fully differential stage to reduce even-order harmonics and minimize common-mode noise interference.

### D. Architecture

Figure 2 shows the architecture of eFDI, conceptually identical to FDI.[12] An FPGA handles the digital devices,

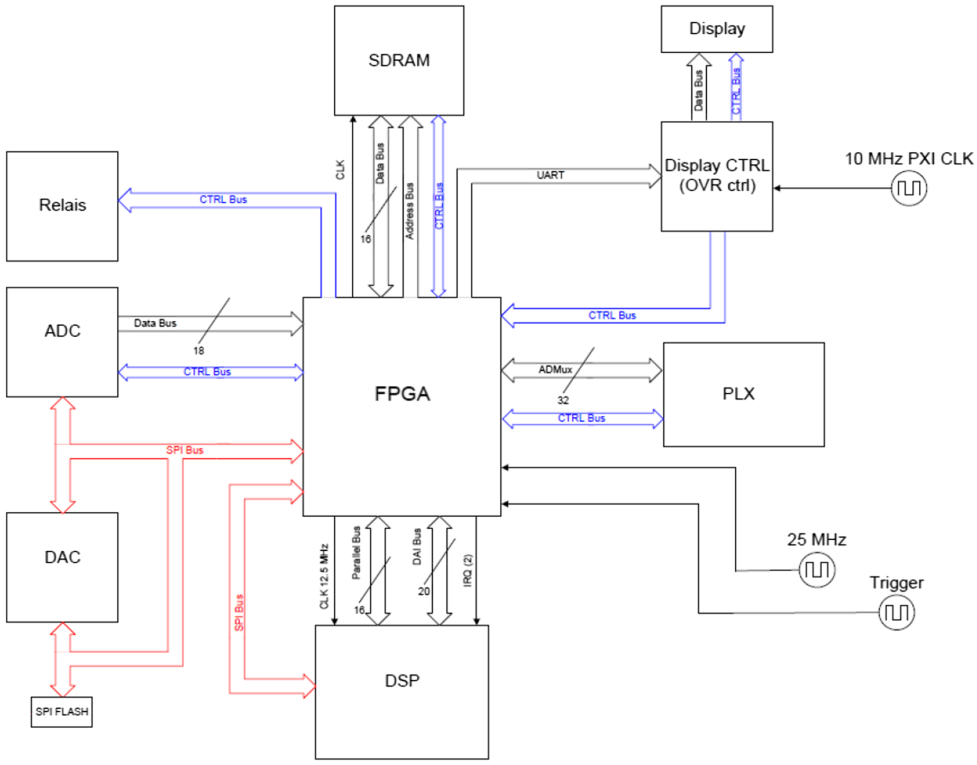


FIG. 2. eFDI architecture.

provides the interface for the board bus, and counts the time stamp pulses aimed at a fine interpolation of the time-domain events. These pulses, generated by a very-low jitter 25-MHz source, allow the time intervals occurring between the ADC clock pulses and the trigger events to be measured by a fine resolution. In the time domain, the main uncertainty sources could arise from the jitter of the Universal Time Counter (UTC) and from the ADC sampling clock. The UTC is generated by a very-low jitter crystal oscillator (0.075 ppm/C). The ADC sampling clock is derived by the same UTC, through high-performance digital counters of the FPGA. For this reason, also the jitter of the ADC sampling clock turns out to be negligible. This was proved in Ref. 45. Furthermore, the FPGA dispatches the Serial Peripheral Interface (SPI) bus between the internal memory, the DAC, and the non volatile flash memory. A Digital Signal Processor (DSP) is in charge of performing the algorithms, carrying out the numerical integration of the samples. The DSP is also in charge of self-calibration procedure by selecting all the available gains and ADC sampling frequency and spanning all the input voltage foreseen by the algorithm. Further, the SDRAM allows ADC sample data buffering.

In extreme synthesis, main design differences with FDI are

1. the *programmable gain amplifier* for signal analog conditioning, based on the operational amplifier of Analog Devices AD8599[44] (AD625 was used in FDI), operating as fully differential amplifier and configured as anti-aliasing filter for noise reduction. Moreover, the AD8599 has a total harmonic distortion (THD) of −120 dB (vs −98 dB of AD625[46]), at 1 kHz with a gain of 1, and is not influenced by input impedance. Thus, AD8599 turns out to be suitable for amplifying signals on different sensing coils. Finally, it is also a more robust component with a simpler operation circuit;
2. *self-calibration*, exploiting a couple of 20-bit, 1-LSB INL DACs (AD5791[40] by Analog Devices) generating differential inputs, in spite of a complex resistor networks and an analog multiplexer;
3. *PXI bus controller*, based on the component PLX 9056, with transmission speed up to 100 MB/s (vs the old PLX 9025 with 2 MB/s), and adding the most important features of direct memory access (DMA) and master bus capability;
4. *time base* at 25 MHz (vs 20 MHz of FDI) allowing a speed-up of the DSP to 200 MHz;
5. *display handler* based on a microcontroller PIC of Microchip instead of a Complex Programmable Logic Device (CPLD), capable of communicating with the DSP and sending more complete information to the user.

### E. Analog signal front-end

Basically eFDI has to maintain the same design challenges of the old version: accuracy requirement of 10 ppm for at least 1 s of integration time with a bandwidth of 100 kHz.[12] Additionally, a lower noise floor and a best input matching for coil signals have to be considered.

Figure 3 highlights the schematic diagram of the analog front-end, composed of 4 main stages:

(a). In the *input stage* (divisor and impedance selection), the input signal (e.g., in the case of the rotating coil at CERN, a 15 V full scale differential output coil[24]) is applied, via LEMO connectors, to the input differential amplifier, which is able to provide 50 Ω or 1 MΩ input impedance and 1/10 or 1/100 division.
(b). The *protection stage* protects the instrument by means of voltage limiting circuits from over-voltage applied by error to the input.
(c). The *programmable gain amplifier* (*PGA*) *stage* is composed by high-performance fully differential amplifiers operating with gains 1, 10, or 100.
(d). The *active filter stage* is based on unity gain, very-low noise and distortion, fully differential amplifier, with optional gain 10. This stage (i) represents the ADC anti-alias filter, implementing a Butterworth structure with configurable cutting frequency; (ii) provides the differential reference for the optimized ADC conversion; and (iii) allows the noise figure to be reduced.

### F. Self-calibration

The FDI self-calibration has two main weaknesses.

1. The algorithm is fully handled by FPGA: this makes difficult changes, aimed at improving or debugging, and makes the correction less precise, owing to the lack of arithmetic and logic unit (ALU).
2. During the calibration steps, the input of the analog front-end is a voltage reference obtained by a resistor network partitioning the 10 V voltage source: this increases the error, arising from the resistor tolerance and ratios, and makes the calibration highly dependent by the temperature despite the adoption of high-quality resistors (0.01%).

The eFDI self-calibration design is mainly focused to provide high-performance voltage references for the input range: a 10 V, 1.09 ppm/°C, 6 ppm/1000 h source reference, applied to a mutually inverted couple of Analog Devices AD5791 20-bits DAC (1 ppm INL, 0.19 LSB long-term linearity, 0.05 ppm/°C),[40] without resistors on the main path, provides the differential calibration signal (Fig. 4). Figure 5 shows the schematic diagram of the voltage reference. The operational amplifiers are used only for signal buffering: the absence of resistors both on the source and the output signal paths allows a high-performance and stable input voltage reference to be provided during the calibration steps. The two DACs are directly programmed by the DSP via SPI bus: a large set of voltage references are allowed and more effective calibration algorithms can be implemented.

The full self-calibration is typically carried out before an official test session on a magnet. The complete procedure, on five gain values (from 0.01 to 100 in logarithmic scale) and for three input impedance values (open, 50 Ω, and 1 MΩ), takes about 20 min. Often, only a partial calibration (for one or two gain and one impedance values) is required with a duration of

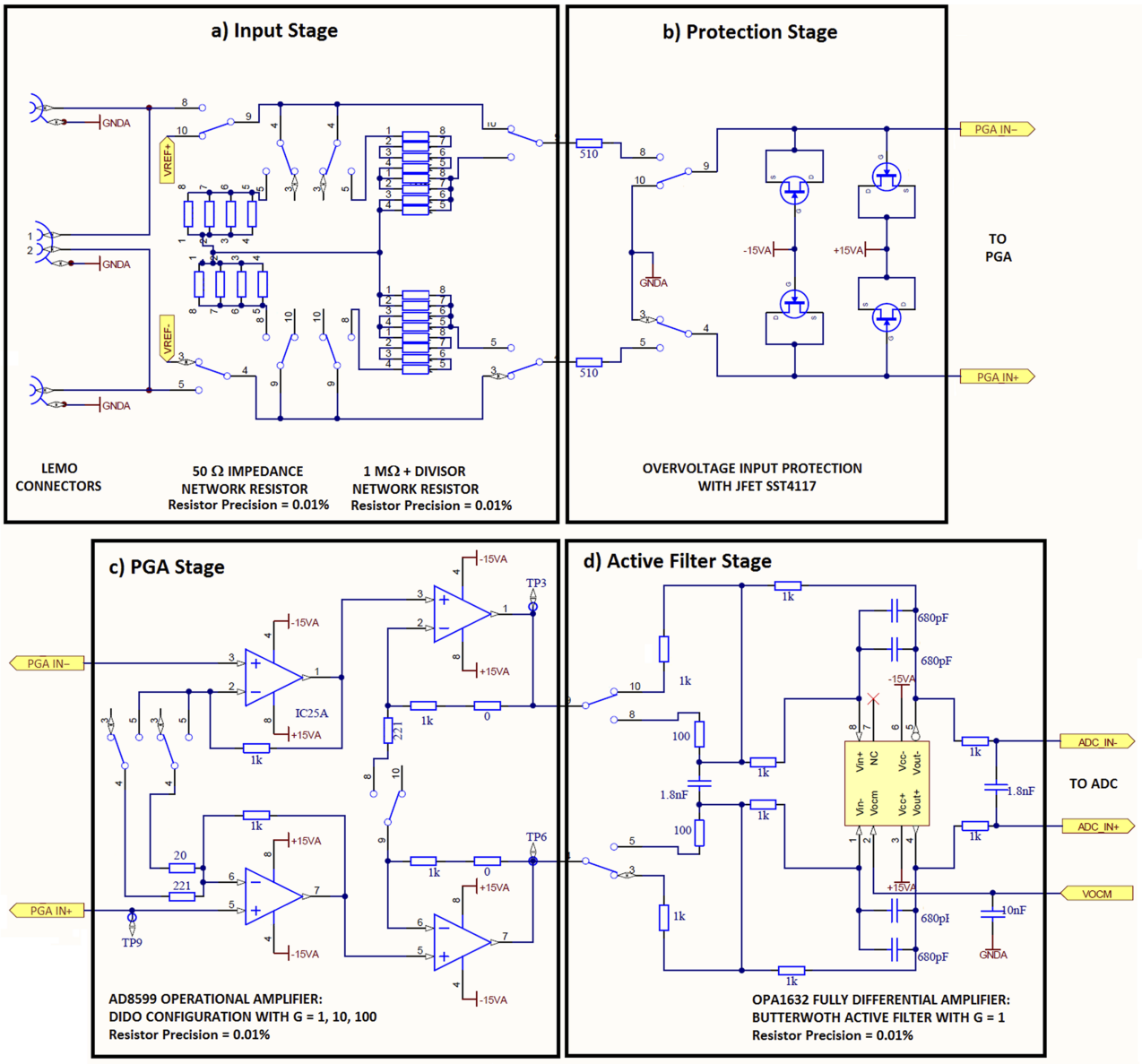


FIG. 3. Schematic diagram of the analog front-end: stages of (a) input, (b) protection, (c) PGA, and (d) active filter.

less than 3 min. The self-calibration is executed on a command invoked by remote through the PXI bus by the test software running on a PC. The corrections are on the mV order for the offset, while for the gain typically the error is $10^{-4}$ before and $10^{-5}$ after the correction.

### G. Digital bus interface

PXI is a rugged PC-based platform which combines the PCI electrical-bus features with the modular, Eurocard packaging of Compact PCI, adding some special synchronization features.[41] FDI is a PXI instrument operating on a 32 bit bus at 33 MHz. The theoretical maximum throughput should be 132 MB/s, and the measured value results less than 10 MB/s.[12] This is mainly due to (i) the bus communication architecture, (ii) the single-mode access, (iii) lack of DMA, and (iv) a non optimized local bus.

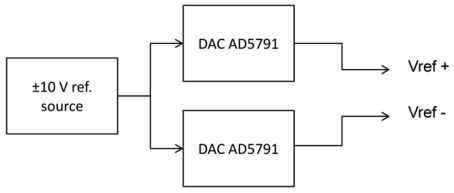


FIG. 4. Self-calibration block diagram.

The eFDI bus communication design is based on the most recent PLX9056 HW accelerator,[43] a general-purpose mastering device available for generic 32-bit, up to 66 MHz local bus based designs.

Figure 6 shows the architecture of the eFDI communications. Signals arrive to FPGA and then are routed to DSP and/or to the local bus. The PLX9056 can support DMA for the PC and act as the master of the PXI bus. The following twofold main improvements are provided: (i) the local bus management was optimized and its clock frequency increased up to 40 MHz, and the (ii) DMA master mode is allowed for

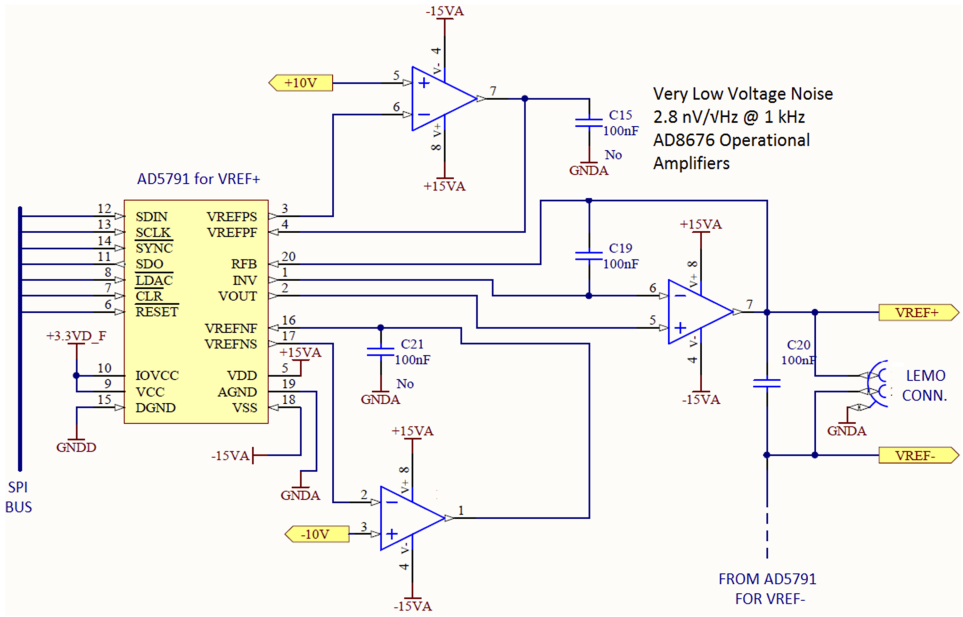


FIG. 5. Schematic diagram of the volt-age reference.

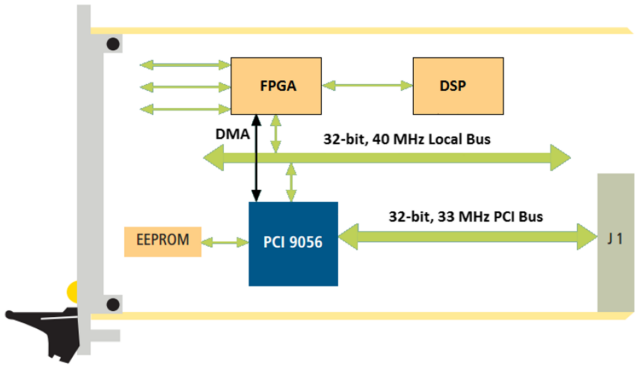


FIG. 6. e-FDI communication architecture.

high-speed direct data transfer from/to PC and FPGA internal DPRAM.

## III. EXPERIMENTAL RESULTS

Figure 7 shows the first eFDI prototype realized for testing purposes. The main performance of both the analog front-end and the self-calibration has been measured, as well as the data throughput has been tested. The first set of the reported tests (*analog front-end tests*) aims at assessing the performance of the analog chain in different points by acquiring the signals with an external acquisition card. In particular, the performance improvement of the instrument is estimated by carrying out dynamic tests and by assessing the SINAD (signal-to-noise and distortion ratio) and the THD. Further tests (*integrator tests*) were carried out to evaluate the prototype acquisition performance by using the on-board ADC. Then, tests (*throughput tests*) of data transmission speed to the PC were carried out. The self-calibration errors are assessed (*self-calibration tests*). Finally, (*comparison with state-of-the-art integrators*) results of performance comparison of the eFDI prototype with FDI and PDI are highlighted too.

### A. Measurement setup

A metrological station (Fig. 8) was set up in order to carry out tests on eFDI, PDI, and FDI. The station is based on a rack ADLINK to host the eFDI and one PCI-PXI bridge card, a standard PC to host the second PCI-PXI bridge card, a calibrator STANFORD DS360 as a reference sine wave generator, and an 18-bit data acquisition card NI USB-6289 by National Instruments. Software applications were developed in C++ and Matlab.

### B. Analog front-end tests

A first set of tests was carried out to verify the signal degradation along the analog chain. A reference sine wave was generated and measured by the NI USB-6289. The signal was analyzed (i) at the output of the first stage of the PGA, at the dedicated test points TP25-TP9 (Fig. 3); (ii) at the output of the second stage of the PGA, before the active filter, at the dedicated test points TP3-TP6 (Fig. 3); and (iii) at the output


FIG. 7. eFDI prototype.

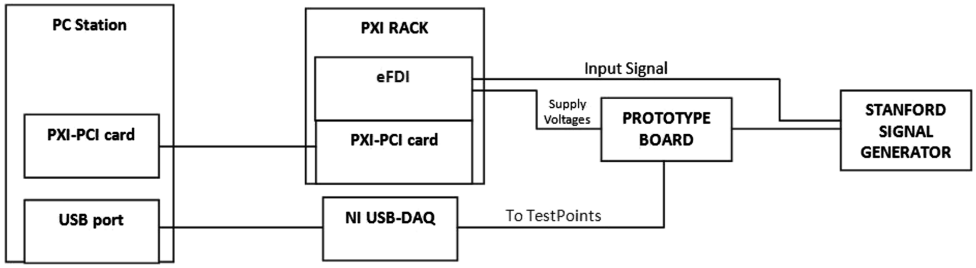


FIG. 8. Measurement setup.

of the analog front-end, that is after the active filter, just before the ADC (AD7634[47]).

An example of the digitized amplitude spectra before (data in black) and after (in blue) the active filter for a sine wave input of 5 Vpp at 63 Hz with the amplifier set to unity gain is depicted in Fig. 9(a). As expected, the noise floor decreases after the low-pass filter (blue). The harmonic distortion, not affected by the amplifiers, remains constant and more visible once the noise is reduced. The resulting SINAD after the filter is 92 dB. In Fig. 9(b), also the output signal of the reference data acquisition NI DAQ-USB is highlighted in red.

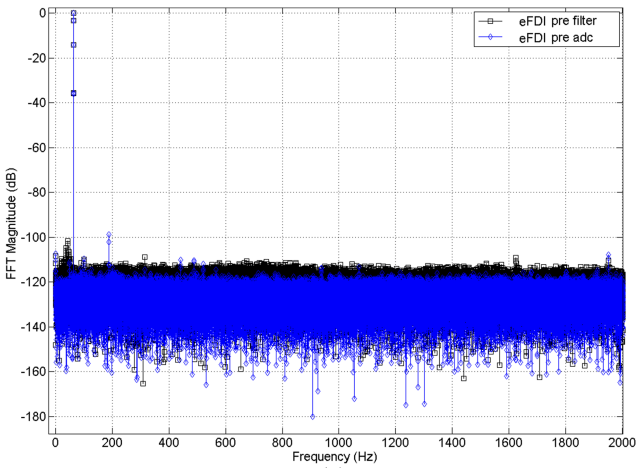


FIG. 9. Amplitude spectrum of the signal before (black) and after (blue) the active filter (just before the ADC) assessed by a 18-bit reference data acquisition system NI DAQ-USB, amplitude 5 Vpp, sampling rate 20 kS/s, time window 30 s (N = 600.000), window Blackman-Harris (resulting SINAD: 82 dB): for an input signal frequency of (a) 63 Hz, in the band up to 2000 Hz, and (b) 7 Hz, zoomed over the band up to 300 Hz. In (b), also the output signal of the reference data acquisition NI DAQ-USB is highlighted in red.

### C. Digitization tests

During a second set of tests, the performance of the eFDI prototype was evaluated in digitizer working mode, that is, by including also the on-board ADC, and by analyzing the raw digitized codes. In Fig. 10, the spectrum of the ADC codes (gain 1, 13 Hz, 5 Vpp) is shown. The resulting SINAD is 88 dB, which is compatible with the results obtained by using the acquisition board. Higher harmonics are visible, in particular, the second and the third ones, and some spurious frequencies as well. They originated mainly from noise at the board level and from the PGA. However, for a unitary gain and for low-test frequency, the PGA noise is assumed as negligible.

### D. Integrator tests

A further test series was carried out by oversampling and then decimating the acquisitions through the DSP integration [Fig. 1(c)], that is, in eFDI integration mode. Tests were carried out by varying (i) the amplitude of the sine wave input, in order to evaluate the dynamic linearity, and (ii) oversampling ratio (OSR), to evaluate dynamic performance as integrator.

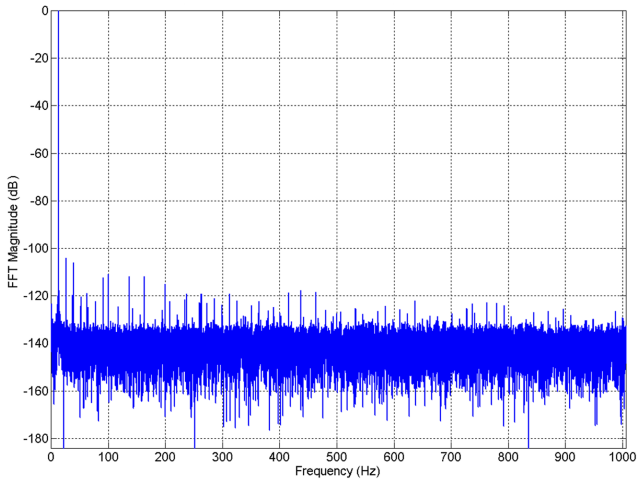


FIG. 10. Amplitude spectrum of ADC codes, input signal frequency 13 Hz, amplitude 5 Vpp, sampling rate 15 kS/s, time window 30 s (N = 450.000), window Blackman-Harris (SINAD: 88 dB).

TABLE II. eFDI integrator performance at varying input amplitude.

| Gain | Vpp (V) | f (Hz) | SNHR (dB)[a] | THD (dB)[b] |
|---|---|---|---|---|
| 0.1 | 30.00 | 7.351 | 101 | −95 |
| 1 | 8.00 | 7.351 | 109 | −96 |
| 10 | 0.80 | 7.351 | 103 | −95 |
| 100 | 0.08 | 7.351 | 96 | −85 |

[a]Total harmonic distortion.
[b]Signal to not harmonic noise ratio.

In Table II, a typical example of eFDI integrator performance in terms of signal-to-not-harmonic-noise ratio (SNHR) and THD is reported at varying input amplitude (0.08, 0.80, 8.00, 30.00) V and correspondingly different gains, for a sine wave input of 7.351 Hz. A satisfying level of linearity can be appreciated at varying gain and input amplitude, corresponding to previous FDI performance.

A set of three different conversion rates was chosen (125, 250, and 500 kS/s) by applying different OSR (125, 250, and 500) in order to give rise to the same sampling frequency. An example of the obtained results (gain 1, input sine wave of 7 Hz and 8 Vpp) is shown for the working mode as a digitizer in Fig. 11(a), and as an integrator, in Fig. 11(b). As expected, again the noise floor decreases at increasing the oversampling ratio (OSR), showing similar results obtained with the NI DAQ. The spectrum of the integrated data is shown in Fig. 12. The typical SINAD of the instrument eFDI used as an integrator is 106 dB, while the typical THD −109 dB. The FFT results of Figs. 11 and 12 highlight, such as expected, a decrease both in noise and in harmonic distortion by increasing the frequency. Considering the application range of the rotating coils, the noise can be considered as negligible. Moreover, the values of SINAD and THD of about 100 dB prove that the basic requirement of a residual gain error of $10^{-5}$ is fulfilled.

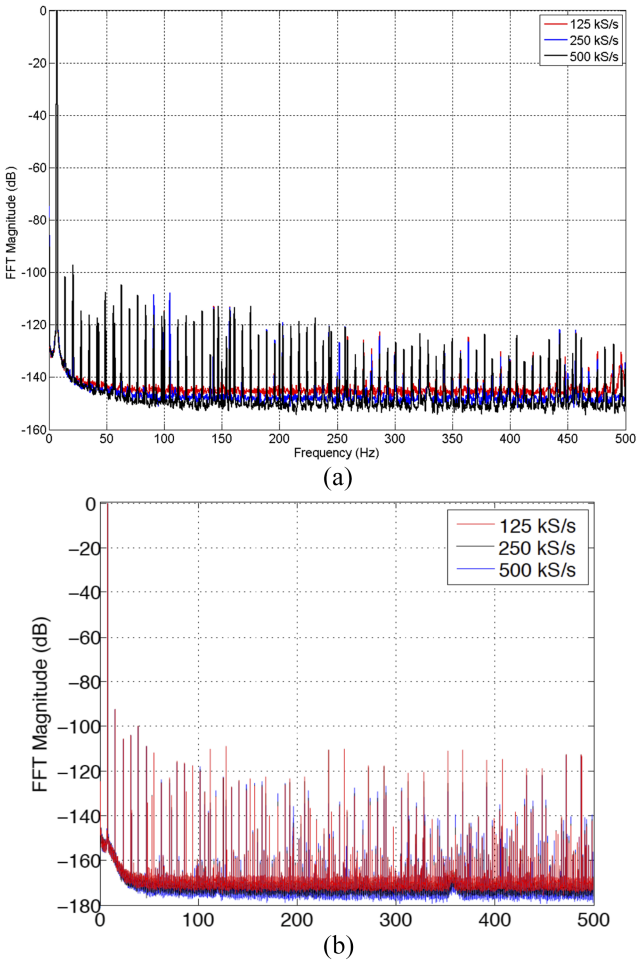


FIG. 11. Amplitude spectrum vs sampling rate for gain 1, input signal frequency 7 Hz, amplitude 8 Vpp, time window 6 s, 30 acquisitions average with N 5.700: (a) digitizer and (b) integrator mode.

## E. Self-calibration tests

The new self-calibration has been evaluated by implementing a standard procedure based on linear regression. Figure 13 shows the results for the linear regression (a) and the normalized residual errors (b) measured in the analog voltage range as a whole. The gain error, offset, and residual error norm were obtained by one-way ANOVA. The reported values are the residuals after calibration. As expected, the residual error is in the order of ppm. The gain error is 0.2% and the offset is 50 $\mu$V. The residual error norm is 2 ppm.

## F. Throughput tests

In this set of tests, data are sent from the instrument to the PC (a PXI controller) via the PXI bus within the rack. Data transmission performance is measured by PLXMon,[48] a software tool provided by the company PLX Technology. In Table III, an example of the corresponding output achieved in a comparative test of eFDI (right) with FDI (left): 15 GB of measured data (integral increments with timestamps) are transferred: (i) for eFDI, in mode DMA burst, in transfer direction DMA slave, in mode local to PCI (i.e., the controller collects the data directory in the on-board acquisition memory), with a local buffer size of 16 kB, and (ii) for FDI, in mode local burst

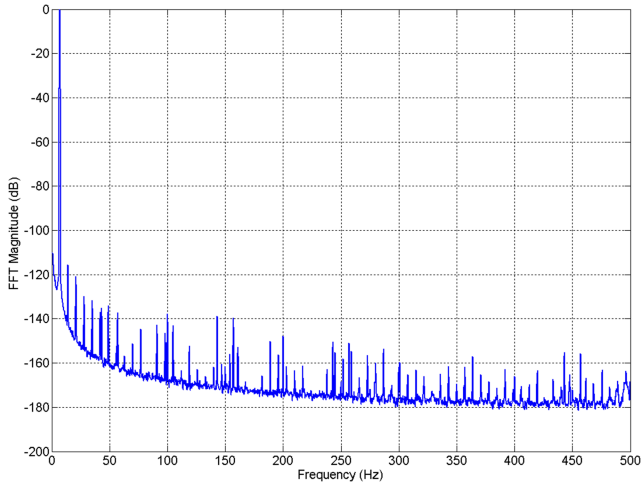


FIG. 12. Amplitude spectrum of the integrated data, for input signal frequency 7 Hz, amplitude 8 Vpp, gain 1, sampling rate 500 kS/s, OSR 500, time window 6 s, and timing average 30 with N 5.700 (SINAD: 106 dB, THD: −109 dB).

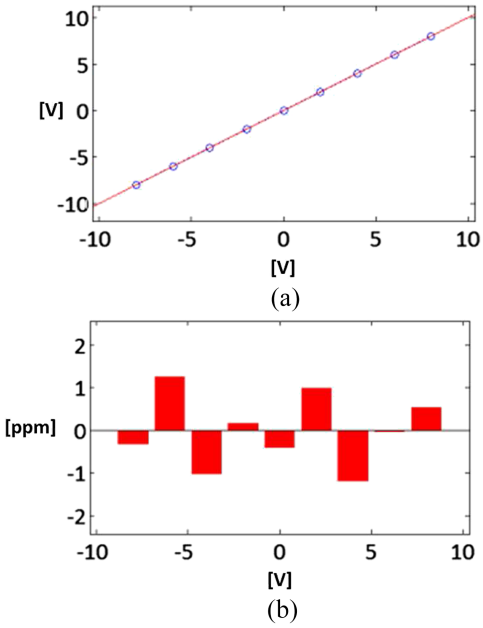


FIG. 13. Self-calibration linear regression: (a) interpolation and (b) residuals.

TABLE III. Comparison between FDI and eFDI throughputs.

| Instrument | Test data size | Buffer size (kB) | Throughput (MB/s) |
|---|---|---|---|
| eFDI | 15 GB | 16 | 107.40 |
| FDI | 45 MB | 16 | 2.82 |

disabled, in the transfer direction read from the device. Obviously, the result of such a test is trivial, owing to the DMA mode of eFDI, but its importance resides in the amount of improvement at the instrumental level: the eFDI achieves an overall rate of 107.40 MB/s, while FDI 2.82 MB/s, namely, an improvement by about 38 times.

Therefore, the master/DMA operation mode of the PCI9056 provides eFDI by a throughput (greater than 100 MB/s), suitable for fast measurements involving several integrators (e.g., transient analysis in testing pulsed magnets[15,49]).

### G. Comparison with state-of-the-art integrators

Table IV shows the comparison results of the three integrator cards: (i) PDI (gain 1000), (ii) FDI with self-calibration (gain 100), and (iii) eFDI prototype (gain 100). A significant compatibility is highlighted in terms of magnetic flux density results (less than 10 ppm with PDI).

TABLE IV. Comparison between PDI, FDI, and eFDI measurements of magnetic field strength (Gdl: integrated gradient).

| Instrument | Gdl (Tm/m)[a] | 1-sigma (ppm) | Difference vs PDI |
|---|---|---|---|
| PDI | 50.995 | 502 | ... |
| FDI | 50.840 | 407 | $-3.04^{-3}$ |
| eFDI | 51.000 | 421 | $8.87^{-5}$ |

[a]Average.

## IV. CONCLUSIONS

An enhanced Fast Digital Integrator (e-FDI) was conceived and prototyped to satisfy the new requirements arising from current on-field exploitation of the previous integrator FDI in magnetic measurements for particle accelerators at CERN. In particular, the new design faced drawbacks related to self-calibration for residual gain and offset errors, and measurement throughput by new analog front-end, self-calibration, and digital bus management.

A metrological characterization of the pre-series eFDI prototypes was carried out in order to assess its performance and design goal's achievement. The typical SINAD of the eFDI used as an integrator was 106 dB, while the typical THD was −109 dB. This reduced noise floor allows signal harmonic analysis also at reduced OSR, suitable for such an application field of state-of-the-art magnetic measurements for particle accelerators. The improved self-calibration procedure provided results comparable with laboratory-calibrated systems. The throughput is increased by about 40 times. Finally, the e-FDI shows significant compatibility in common working conditions and operating ranges with FDI and PDI.

Further work will be devoted to assess stability and temperature behavior.

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