Proof of principle of an on-line digitizer with ±18 ppm repeatability and 1.2 μs real-time delay for power converters control loop

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Proof of principle of an on-line digitizer with ±18 ppm repeatability and 1.2 μs real-time delay for power converters control loop

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Abstract: The proof of principle of an on-line digitizer designed to be integrated into the digital control loop of a high-voltage modulator for ultra-repeatable power converters is presented. The presented selective analogue zoom allows digitizing with ±18 ppm repeatability the voltage around the nominal level (10 V±1 V) and, at the same time, the initial transients with relaxed performance. In addition, in order not to jeopardize the digital control loop stability, the whole digitizing system has to introduce a low real-time delay; this is assessed to be less than 1.2 μs. Initially, the specifications of the real-time control are presented and translated into data acquisition requirements. Then, the main design choices of the digitizer are discussed and *Pspice* simulation results are reported to validate the concept design. Finally, experimental results of a validation case study developed for the power converter designed at *ETH* Zurich and University of Laval for the new linear particle accelerator under study at *CERN*, the Compact LInear Collider *CLIC*, are reported and compared with the simulation outcomes.

Keywords: Analogue electronic circuits; Data acquisition circuits; Data acquisition concepts; Control and monitor systems online

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1 Introduction

Real-time data acquisition systems are used in many industrial or research situations which require monitoring and control operations [1, 2] and are nowadays considered as a fundamental part of digital control loops [3]. They provide, by means of a feedback, a suitable adjustment to the loop controller in order to reach the required performance. For this reason, there is a new-found interest in this line of research in fields ranging from military [4] to electronic controls in automotive [5]. This is the case, for example, in effective energy management of fuel cell powered electric vehicles [6], and even heavy trucks [7]. The main challenge in designing an efficient digital control system is to meet both metrological requirements and time constraints imposed by the specific application. Some new applications require acquisition systems with precision in the order of few tens of parts per million, capable of digitizing and providing data to the controller within a very short delay, in the order of few μs. This is the case, for example, of smart power flow management between separate energy storage units [8] and high-performance electric vehicles [9].

In this context, challenging applications are provided by a new generation of power converters, using enhanced digital loop methods [10]. Such methods allow to (i) add new features, (ii) improve performance, and (iii) increase flexibility, while keeping the cost low [11]. High-performance pulsed power converters are increasingly used for discontinuous loads where significant power savings are achievable by using pulsed power converters instead of DC ones [12].

This is the case of the new linear electron-positron particle accelerator currently under study at *CERN*, the Compact LInear Collider (*CLIC*) [13]. It will allow collisions up to several TeV, exploring energy regions never reached before, thanks to its unprecedented combination of high energy and experiment precision. In order to reach the desired energy level, together with reasonable power consumption from the electrical grid [14], *CLIC* needs for power converters [15] with a pulsed power [16] repeatable in the order of few tens of ppm [15]. For this purpose, a high-voltage modulator is currently being designed by the laboratory for high-power electronics at *ETH* Zurich (CH) [17] and the *LEEPCI* Laval (CA) [18]. This is a typical example of new generation power converters requiring a real-time digitizer with delay in the order of few μs over a bandwidth of less than 1 MHz, with repeatability performance in the order of few ppm.

In this paper, the design and the experimental proof of principle of a ±18 ppm repeatable digitizer, with real-time delay less than 1.2 μs on 11 V of full-scale, is presented (more details on the overall metrological aspects of the project can be found in [19]). In section 2, the system

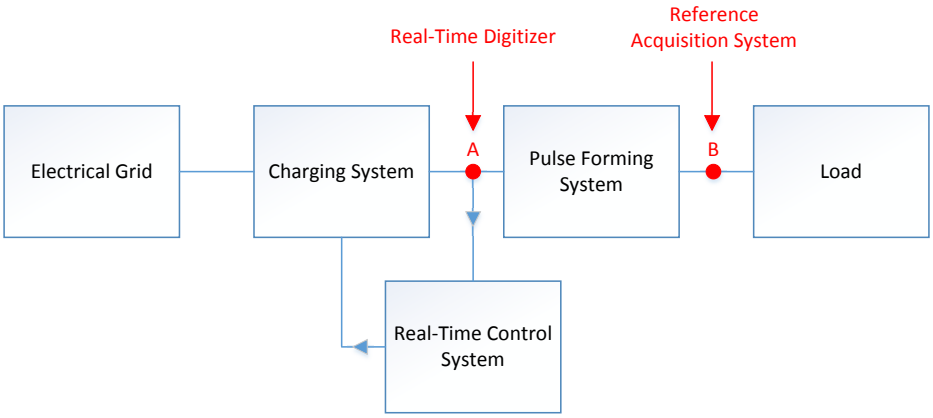

Figure 1. Typical topology of a pulsed power converter.

requirements are stated, whereas in section 3, the working principle and the concept design are highlighted. In section 4, the design choices are detailed and the circuital realization of the prototype for a validation case study at $CERN$ of the power converter for $CLIC$, is presented. Finally, in sections 5 and 6, the simulation and experimental results, respectively, are presented and discussed.

2 Requirements

2.1 Measurand

In figure 1, the typical topology of a pulsed power converter is sketched. The two nodes A and B denote the two points where measurement systems are needed. In point B, a reference measurement system is required for assessing the final performance of the converter [20]. In point A, the real-time digitizing system, discussed in this work, allows an active control of the charging system output voltage.

Thus, the voltage in point A is the signal to be digitized by the proposed instrument. As shown in figure 2, the typical measurand waveform is characterized by different regions: (i) a $Pre-charge$, with an initial ramp up where the charging system reaches the nominal voltage V_N, (ii) a $Pulse$, where the modulator generates the pulse ideally keeping the voltage constant, and (iii) a $Recharge$, where the nominal voltage out of the charging system is restored. In the $Pre-charge$ and $Recharge$ regions, the flat-top of the high-voltage signal might have variations ($\pm\Delta$) with respect to the nominal voltage. The measurand waveform of figure 2 is firstly transduced into low voltage by a high-voltage divider. Thus, the flat-top is reduced to 10 V, typically. For this reason, all the issues related to high voltage measurements are not discussed in this work.

One of most crucial design challenges for the digitizer arises from the simultaneous satisfaction of the performance requirements (i) on the high state, during the $Pulse$, and (ii) on a wide-range signal in real time, during the other two regions of $Pre-charge$ and $Recharge$. Furthermore, a switched-mode power converter generates a switching noise superimposed on the measurand that must not jeopardize the final performance of the digitizer.

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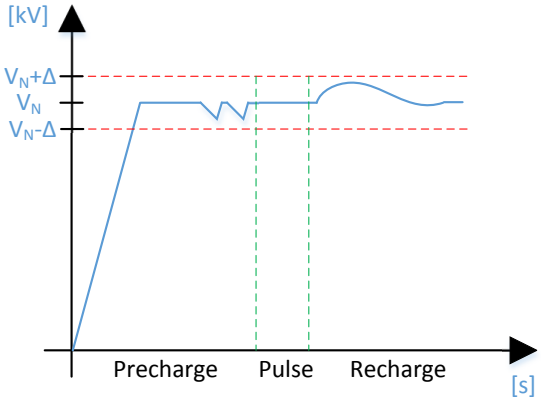

Figure 2. Output voltage waveform of the charging system.

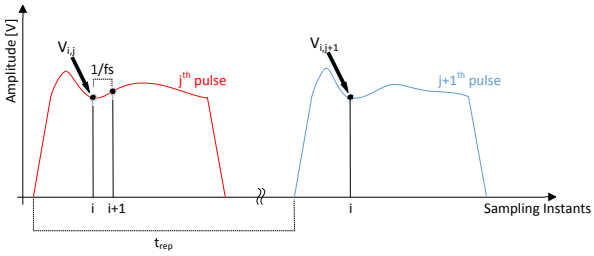

Figure 3. Pulse-to-pulse repeatability definition.

2.2 Repeatability

The digitizer has to guarantee a typical repeatability of the power converter modulator in the order of ±50 ∼ 100 ppm of full-scale during the pulse. In industrial applications, discussed in [20], a Pulse-to-Pulse Repeatability (PPR) is defined as:

$$PPR = \max |V_{i,j} - V_{i,j+1}| \tag{2.1}$$

where $V_{i,j}$ and $V_{i,j+1}$, illustrated in figure 3, are the instantaneous voltage values in the *same* (in equivalent time) sampling instant i between two consecutive pulses on the secondary side of the modulator, namely j^{th} and $j^{th} + 1$. For the charging system of the power converter, this definition applies to the region $Pulse$. Thus, the digitizer PPR is to be set in the order of 50 ∼ 100 ppm. It has been studied in [20] that if the digitizer has a suitable stability within the pulses period, the noise is the only factor affecting repeatability, and thus all the long-term effects (e.g. temperature drift) can be neglected.

2.3 Throughput and bandwidth

When the digital control of a switching power converter has to be designed, a typical choice is to close the control loop at the switching frequency ($f_{\text{loop}} = f_{\text{switching}}$). Thus, the digitizer must deliver one sample at each control-loop period (T_{loop}), defining the throughput as Throughput = $f_{\text{loop}} = \frac{1}{T_{\text{loop}}}$. The digitizer bandwidth should be limited to less than $\frac{f_{\text{loop}}}{2}$ to cope with aliasing. In addition, the

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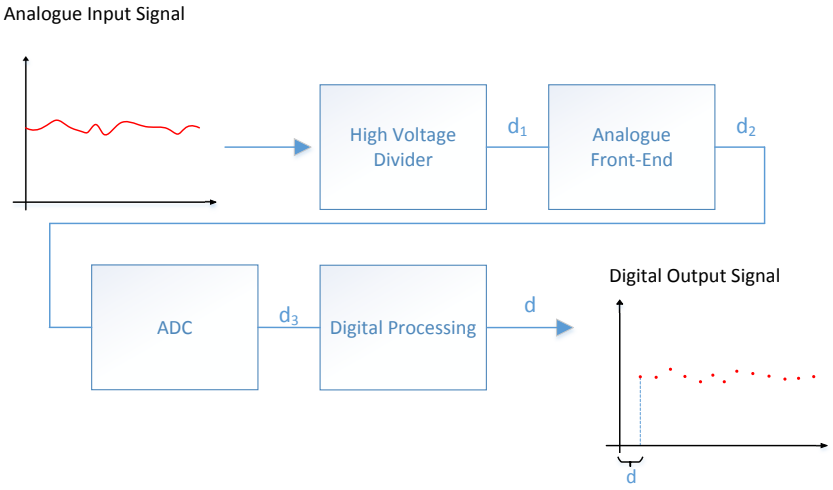

Figure 4. Definition of delay in a power converter real-time data acquisition.

power switches of a switched pulsed converter (e.g. IGBT) working at $f_{\text{switching}} = f_{\text{loop}}$, generate a relevant ripple at that frequency (and harmonics). This has to be rejected effectively in order not to jeopardize the final performance of the digitizer, thus an adequate filtering strategy has to be adopted.

2.4 Delay

Delay is one of the most important parameters of a digital control loop. A total delay d is specified for the whole measurement chain sketched in figure 4 (from the high-voltage divider up to the digital processing used for signal reconstruction). In the following, for the sake of simplicity, "delay" is defined as $\tau_g(0)$, with $\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega}$, being the group delay. In order to keep the total delay within one loop period, 70 % of T_{loop} is usually intended for the measurement chain delay (d) whereas the remaining 30 % is allocated for data communication. This is a challenging specification if typical values of $d < 1$ μs are needed in combination with an overall bandwidth in the order of few hundreds of kHz.

3 Concept design

In this section, the design of the proposed digitizer (whose working principle is sketched in figure 5) is discussed with respect to the defined requirements. The whole digitizer is composed by a high-voltage divider, an analogue front-end, and an ADC based system.

3.1 Basic principle

During the region $Pre - charge$, where no particular precision is required ($< \pm 1$ %), the switch S_1 allows the input signal to be subtracted from itself in order to obtain (ideally) a null signal on the upper branch of figure 5. Simultaneously, a wide-range ADC (ADC_2) digitizes the input signal, by carrying out a coarse measurement of the initial ramp. When the ramp is over (this event is identified by an external trigger provided by the modulator), the switch commutes toward

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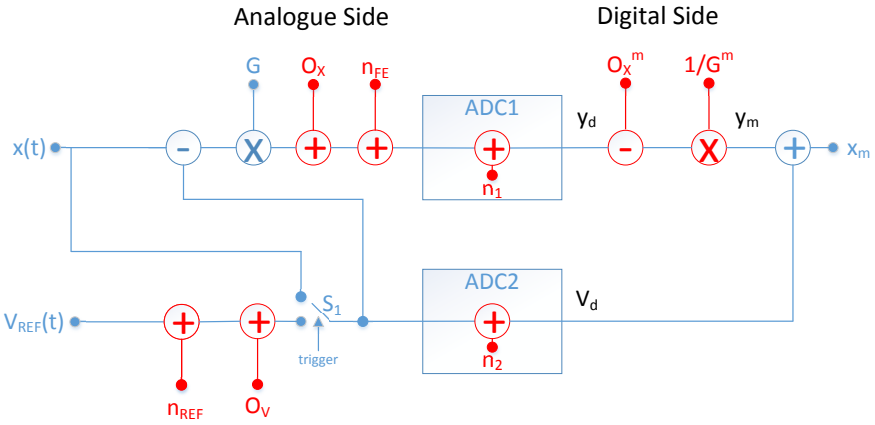

Figure 5. Block diagram of the real-time digitizer.

an internal reference voltage, $V_{\mathrm{REF}} = 10\,\mathrm{V}$. This is subtracted from the signal (downstream of the voltage divider) in order (i) to center its high state around zero, and then (ii) to amplify by a factor G only the part where a high precision is required to best fit ADC_1 range.

Down-stream of these two operations, unwanted offset (O_x in figure 5) and gain errors will arise from all the possible analogue components. Gain and offset corrections are applied digitally in order to reconstruct the original signal properly. Real-time delay is a constraining parameter in digital control applications, therefore both $ADCs$ were based on SAR architectures. SAR and $Flash\ ADCs$ have the lowest latency (1-clock cycle) but the latter are less suitable for high-precision applications.

3.2 Full signal reconstruction

During operations, both the conditioned input signal x and the internal reference DC voltage V_{REF} are digitized. These two signals are affected by the noise of (i) the front-end (n_{FE}), (ii) the reference (n_{REF}), and (iii) the two $ADCs$ quantization, respectively n_1 and n_2 (assuming an ideal additive noise model for the $ADCs$). In order to reconstruct the original input signal x, the offset and gain errors of the analogue path (Ov,Ox, and G) have to be measured and digitally compensated (Ox^m and G^m). The signals y_m and V_d are the digitized outcomes of the two digitizer branches in figure 5 summed to achieve the result x_m:

$$x_m = \frac{[x - (V_{\mathrm{REF}} + n_{\mathrm{REF}} + Ov)] \cdot G + Ox + n_{\mathrm{FE}} + n_1 - Ox^m}{G^m} + \\ + V_{\mathrm{REF}} + n_{\mathrm{REF}} + Ov + n_2 \tag{3.1}$$

Actual gain G^m and offset $Ox^m = Ox$ can be accurately measured so that $G^m = G$ and $Ox^m = Ox$, (full uncertainty estimation not discussed here) and:

$$x_m = x - V_{\mathrm{REF}} - n_{\mathrm{REF}} - Ov + \frac{n_{\mathrm{FE}} + n_1}{G^m} + \\ + V_{\mathrm{REF}} + Ov + n_2 = x + \left(\frac{n_{\mathrm{FE}} + n_1}{G^m}\right) + (n_{\mathrm{REF}} + n_2) \tag{3.2}$$

where all the deterministic errors were already compensated.

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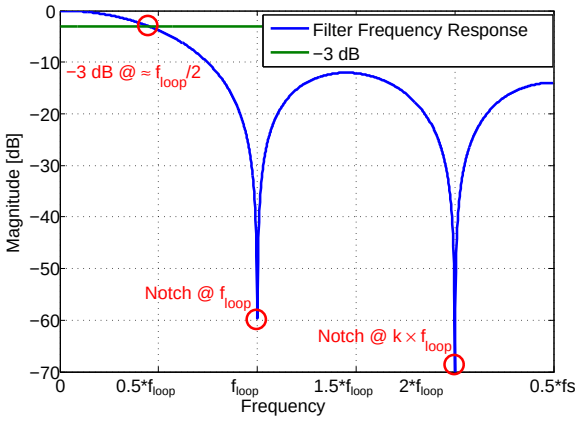

Figure 6. Frequency response of the average 4^{th} order FIR filter.

In conclusion, particular attention should be paid to (i) accurately measure gain and offset of the digitizer as a whole (analogue front-end plus ADCs) for proper compensation, (ii) design a low-noise front-end in order to keep $\frac{n_{\mathrm{FE}}}{G}$ as low as possible, (iii) heavily filter n_{REF}, and (iv) use high-resolution $ADCs$ such that $\frac{n_1}{G}$ and n_2 meet the specs. It is worth nothing that as G increases, both the contributions of the analogue front-end and the ADC_1 decrease; thus, at this stage, the higher G, the lower the overall noise is.

3.3 Sampling and filtering strategy

The ripple produced by the power switch of the converter has to be rejected using an adequate filtering strategy. For this purpose, oversampling [21], filtering, and decimation are exploited, by selecting an adequate sampling rate $f_s = N \cdot f_{\mathrm{loop}}$, where N is the oversampling ratio.

Aliasing is made negligible by the analogue filter by mitigating the effect of noise in the range of frequencies folding in baseband. In addition, oversampling has the advantage of relaxing the analogue anti-aliasing filter requirements. In a high-voltage modulator, the upstream divider, assumed as a first-order filter with few MHz bandwidth, already plays a role in the analogue anti-aliasing filtering strategy, by introducing additional attenuation and increasing the delay.

For digital filtering, a simple average filter, belonging to the class of linear-phase *FIRs*, is foreseen. In this way, whichever oversampling ratio is chosen, the relative filter will show a notch at f_{loop} and harmonics, ideally eliminating the switching ripple. In figure 6, the frequency response of a 4^{th} order average filter ($N = 5$) is depicted to highlight its notches. The group delay introduced by such filters can be estimated as:

$$d_{\mathrm{digital}} = \frac{N-1}{2N f_{\mathrm{loop}}} \tag{3.3}$$

where N is the number of coefficients.

3.4 ADC noise vs analogue noise

Equation (3.2) states the dependence of the reconstruction quality of x on both the analogue (n_{FE} and n_{REF}) and the digital noise (n_1 and n_2).

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In equation (3.4), the definition of the worst-case PPR, namely the Worst-Case Repeatability (WCR), is reported.

$$WCR = \max_j \left(PPR_j\right) \tag{3.4}$$

In [22], an analytical model describing the statistical distribution of WCR was defined for an instrument affected by Additive White Gaussian Noise ($AWGN$). This happens typically when an analogue uncertainty source modeled as $AWGN$ is significantly dominant with respect to the quantization noise of the ADC, assumed to be uniformly distributed between $-\frac{\Delta}{2}$ and $\frac{\Delta}{2}$, where Δ is the $ADC\ LSB$. Conversely, if the quantization noise is dominant with respect to analogue uncertainty sources, the WCR cannot be higher than Δ itself. In the following, the most important uncertainty sources are discussed.

3.4.1 $ADCs$ quantization noise, n_1 and n_2

ADC_1 has to digitize the $high - state$ signal only. ADC_1 samples at $N \cdot f_{\text{loop}}$, then the output is filtered and decimated (average of N samples) down to f_{loop} in order to enhance effective resolution. The rms value of the quantization noise n_1 is attenuated by $\sqrt{N}$ thus an equivalent down-sampled quantization noise with rms value $\sigma_{\overline{n}_1} = \frac{\sigma_{n_1}}{\sqrt{N}}$ is considered.

Therefore, the "equivalent" rms quantization noise and, in turn, an "equivalent" LSB, are defined:

$$\begin{aligned} \sigma_{\overline{n}_1} &= \frac{VS_1}{2^{ENOB_1} \cdot \sqrt{12\,N}} \\ \overline{\Delta}_1 &= \sigma_{\overline{n}_1} \sqrt{12} \end{aligned} \tag{3.5}$$

where VS_1 and $ENOB_1$ are the input Voltage Swing and Effective Number Of Bits of ADC_1 respectively. Finally, the rms noise referred to input is introduced: $\sigma_{\overline{n}_1'} = \frac{\sigma_{\overline{n}_1}}{G} = \frac{VS_1}{2^{ENOB_1} \cdot G\sqrt{12\,N}}$.

ADC_2 has to digitize the reference voltage V_{REF} and the signal sketched in figure 2 in the $Pre - charge$ region. Analogously as for ADC_1, the "equivalent" rms quantization noise and the "equivalent" LSB are defined as:

$$\begin{aligned} \sigma_{n_2} &= \frac{VS_2}{2^{ENOB_2}\sqrt{12}} \\ \Delta_2 &= \sigma_{n_2}\sqrt{12} \end{aligned} \tag{3.6}$$

3.4.2 Analogue noise

The DC reference voltage to be subtracted from the original signal is affected by the noise n_{REF}. This branch of the front-end does not have constraining requirements in terms of bandwidth, therefore the DC reference voltage can be heavily filtered in order to keep $\sigma_{n_{\text{REF}}}$ negligible with respect to σ_{n_2} (i.e. at least one order of magnitude smaller).

Finally, $\sigma_{\overline{n_1}'}$ is the rms value of the overall noise of the analogue front-end referred to input. A low-noise design for the front-end is indeed one of the main requirements. Given the proposed working principle, also the analogue front-end noise will be filtered and decimated. Analogously as for σ_{n_1}, the equivalent down-sampled noise can be defined as $\sigma_{\overline{n}'_{\text{FE}}} = \frac{\sigma_{n_{\text{FE}}}}{G\sqrt{N}}$. The assumption of a quantization noise dominant with respect to the analogue noise is satisfied by keeping also $\sigma_{\overline{n}'_{\text{FE}}}$ at least one order of magnitude smaller than the total quantization noise (see equation (3.2)).

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3.4.3 Worst-case repeatability

At the required bandwidth, the quantization noises of the two $ADCs$ are expected to be dominant compared to the front-end's noise. Under the assumption of uniformly-distributed quantization noises for the two $ADCs$, a deterministic superior bound for the Worst-Case Repeatability (WCR), defined as the worst expected case of PPR, can be estimated. In fact, from (2.1), the worst-case condition is verified when the j^{th} acquisition is affected by a quantization error $\left(\frac{\overline{\Delta}_1}{2} + \frac{\Delta_2}{2}\right)$ and the $(j+1)^{th}$ by $-\left(\frac{\overline{\Delta}_1}{2} + \frac{\Delta_2}{2}\right)$. Thus, the superior bound can be assessed as:

$$WCR = \overline{\Delta}_1 + \Delta_2. \tag{3.7}$$

4 Case study on CLIC power converter modulators

4.1 The CLIC power converter modulator

A very-challenging case study has been provided in the framework of the new linear electron-positron particle accelerator currently under study at $CERN$, the Compact LInear Collider ($CLIC$) [13]. It will allow collisions up to several TeV, by exploring energy regions never reached before, thanks to its unprecedented combination of high energy and experiment precision. In order to reach the desired energy level, $CLIC$ power converters [15] are required to deliver pulsed power, repeatable in the order of few tens of ppm [15].

For this purpose, a high-voltage modulator is currently under design by the laboratories for high-power electronics at ETH Zurich (CH) [17] and the $LEEPCI$ Laval (CA) [18] (figure 7).

It is composed by a charging system, which, after a region $Pre-charge$, accumulates energy from the grid at a nominal output voltage of 3 kV and an active bouncer which allows to limit the voltage fluctuations to about 10 % of the nominal voltage. The switching unit allows the stored energy to be released during 140 μs, obtaining a pulse train on the primary side of a split-core transformer at a repetition rate of 50 Hz. The charging system output voltage is also regulated by an active bouncer to mitigate the effect of discharge of the capacitors bank during the pulses. Finally, on the secondary side, the pulses are amplified up to 180 kV directly feeding the klystrons.

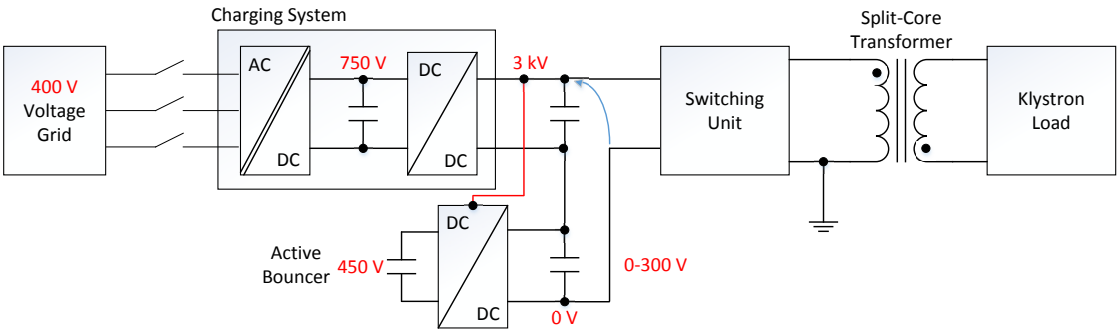

Figure 7. Topology of the high-voltage modulator under design at ETH Zurich [17].

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Table 1. Main requirements of the case study of the power converter modulator for *CLIC* [17, 18].

Parameter	Symbol	Value
Repeatability during Pulse	Rep_p	50 ppm
Repeatability elsewhere	Rep	$< 1\,\%$
Digital filtering order	N	5
Loop frequency	f_{loop}	600 kHz
Sampling frequency	f_s	3 MHz
Bandwidth	BW	200 kHz $< BW <$ 300 kHz
"Alias-free" bandwidth	B_{AF}	$(f_{AF} \rightarrow f_s) = (2.7 \rightarrow 3.0\,\text{MHz})$
Delay	d	$< 1.2\ \mu$s

4.2 The measurement system

A high-voltage divider [23] is used to convert the 3 kV ±300 V into 10 V ±1 V (waveform in figure 2) to be handled by a suitable real-time digitizing system in order to run a digital control loop at $f_{\text{loop}} = 600\,\text{kHz}$. In the concept design, oversampling and decimation are exploited, thus the actual sampling rate is $N \cdot f_{\text{loop}}$. However, the oversampling ratio N, and hence maximum achievable attenuation, is traded against the delay of the digital filter needed to bring the throughput back to f_{loop}. A value of $N = 5$ was chosen for this design. A minimum attenuation of 10 dB at $f_{AF} = N \cdot f_{\text{loop}} - \frac{f_{\text{loop}}}{2}$ was indeed estimated as sufficient, where f_{AF} is the first frequency component folding back to the base-band $\left[0,\ \frac{f_{\text{loop}}}{2}\right]$. In fact, no significant noise components at high frequency are expected, except from switching harmonics, suitably rejected by the *notches* of the moving average filter. In table 1, the main requirements for the real-time digitizer for the *CLIC* case study [17, 18] are summarized.

4.3 The choice of the ADCs

ADC_1 has to sample at $5 \cdot 600\,\text{kS/s} = 3\,\text{MS/s}$. *AD*7625 is a 16-bit *SAR ADC* with a declared *SINAD* of 92 dB which corresponds to an Effective Number Of Bits, $ENOB_1 \approx 14.9$. The input Voltage Swing is $VS_1 = \pm 4.096\,\text{V}$, thus its "equivalent" LSB can be calculated according to equation (3.6). It is worth noting that, given the expected signal swing of ±1 V (downstream of the voltage divider) and the maximum input Voltage Swing of ±4.096 V allowed by the *ADC*, the gain applied by the analogue front-end is limited to $G = 4\,\text{V/V}$ (in order to leave some margin for unexpected over-voltages). Thus, the "equivalent" LSB can be calculated to be: $\overline{\Delta}_1 \approx 30\,\mu\text{V}$, ($\sigma_{\overline{n}_1'} \approx 0.9\,\text{ppm}$).

ADC_2 has to digitize at $f_{\text{loop}} = 600\,\text{kS/s}$ the reference voltage V_{REF} and the $Pre-charge$ signal on a 10 V range. *AD*7634 is a 18−bit *SAR ADC* with a SINAD of 100 dB ($ENOB_2 \approx 16.3$) and, consequently, the "equivalent" LSB is about $\Delta_2 \approx 124\,\mu\text{V}$, ($\sigma_{n_2} \approx 3.6\,\text{ppm}$).

In these conditions, equation (3.7) gives a *WCR* superior bound of roughly 15.4 ppm which is comfortably lower than the requirement of 50 ppm.

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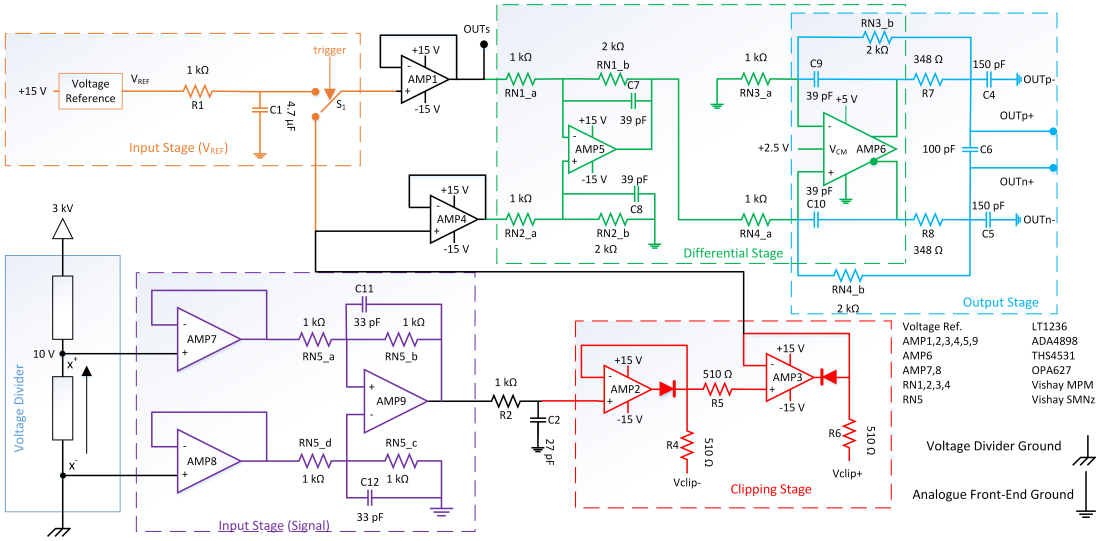

Figure 8. Analogue front-end schematics.

4.4 Physical design of the analogue front-end

In figure 8, the schematics of the proposed analogue front-end, the real core of the proposed digitizer, are depicted. The main stages are described in the following.

4.4.1 Input stage (V_{REF})

On the upper branch in figure 8 (orange dashed rectangle), the internal reference voltage (V_{REF}) is realized by means of the voltage reference Linear Technologies $LT1236$. The low-pass filter R_1C_1 has a cut-off of about 30 Hz. The switch S_1 selects the corresponding line to be subtracted from the signal according to the particular region of the input signal ($Pre-charge$ or $Pulse$ in figure 2). The input signal is then buffered by $AMP1$.

4.4.2 Input stage (signal)

On the lower branch in figure 8 (violet dashed rectangle), a differential sensing circuit is used on the signal input in order to [20, 24]:

- Decouple the voltage divider from the analogue front-end by means of two input buffers;
- Reject the Common Mode Voltage between the analogue front-end and the voltage divider arising from the ground loop related to separated grounds, by means of a suitable unity gain difference amplifier. As a matter of fact, the voltage divider and the measurement system will be installed into two separate racks, therefore the relative ground voltages might be significantly different.

In addition, a 2^{nd} order low-pass filter ($R_{N5b}C_{11}R_{N5c}C_{12}R_2C_2$) represents the first stage of the anti-aliasing filter described in (3.3) (the stage "zero" of the anti-aliasing filter is represented by the upstream voltage divider).

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4.4.3 Clipping stage

A fast clipping circuit (red dashed rectangle in figure 8), based on the cascade of two $ADA4898$ [25] in super-diode configuration, protects the input stage of ADC_1. During the region of $Pre-charge$, the low-side clipping is deactivated by setting the voltage $Vclip-$ to ground.

4.4.4 Differential stage

Another difference amplifier is used to translate the input signal (green dashed rectangle in figure 8) around zero, by subtracting the reference voltage (upper branch in figure 8), and to apply a gain $G_1 = 2\,\mathrm{V/V}$. Finally, a Fully Differential Amplifier (model $THS4531$ performs single-ended to differential conversion and amplifies the signal by a factor $G_2 = 2\,\mathrm{V/V}$. Two separate differential stages are needed because the FDA only allows a unipolar supply voltage of, at most, 5 V. This means that it cannot handle 10 V input signals. With these two amplifying stages, a total gain $G = 4\,\mathrm{V/V}$ is obtained in order to bring the ±1 V fluctuations almost to the full-scale of ADC_1 (the actual full-scale is ±4.096 V). The resistor networks $RN_{1,2,3,4}$ are the Vishay MPM series, which guarantee a good gain accuracy, given the low relative tolerance resistors of 0.05 %.

4.4.5 Output stage

The last stage in figure 8 completes the analogue anti-aliasing filter described in (3.3) (light blue dashed rectangle). In figure 8, the reported values for all the resistors and capacitors involved in the filter are chosen in order to have at least 10 dB of attenuation at $f_{AF} = N \cdot f_{\mathrm{loop}} - \frac{f_{\mathrm{loop}}}{2} = 2.7\,\mathrm{MHz}$.

5 Numerical results

In this section, the above design is validated by comparing the requirements stated in section 2 with the simulation results obtained on a Pspice model. In particular, noise and bandwidth of the analogue front-end are simulated in 5.1, whereas the expected delay and Worst-Case Repeatability (WCR) of the whole digitizer are discussed in 5.2 and 5.3 respectively.

5.1 Noise and bandwidth

Two simulation campaigns were carried out to verify bandwidth and noise performance.

In the first simulation, the noise introduced by the analogue front-end was assessed. The contributions of all the components sketched in figure 8 are taken into account. The results, depicted in figure 9 (dotted curve), show an rms noise value of about $\sigma_{n'_{\mathrm{FE}}} \approx 3.2\,\mathrm{ppm}$ referred to input (RTI) which does not take into account the attenuation of $1/\sqrt{N}$ introduced by the digital filtering.

In the second simulation, the −3 dB bandwidth of the analogue front-end of the proposed on-line digitizer was assessed. In figure 9, the simulation results are depicted showing that the −3 dB bandwidth is higher than 1 MHz, while an attenuation of more than 10 dB is obtained at $f_{AF} = 2.7\,\mathrm{MHz}$, as stated in section 4.

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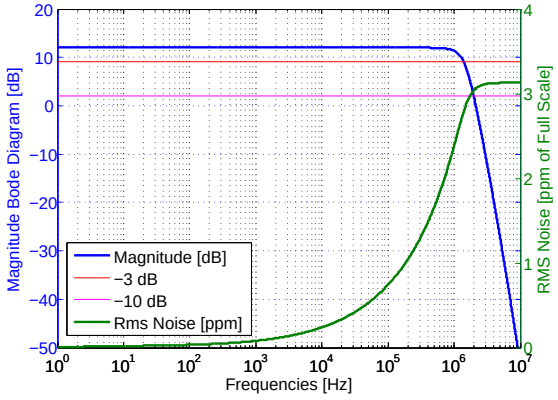

Figure 9. Magnitude bode diagram and rms noise.

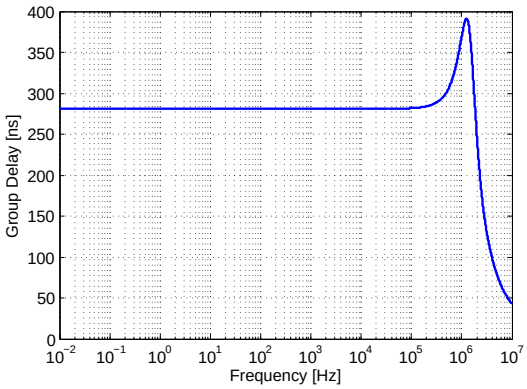

Figure 10. Group delay.

Table 2. Expected delay.

Source	Value [ns]
High-voltage divider	160
Analogue front-end	280
ADC	40
Digital filtering	670
Total	**1150**

5.2 Delay

The group delay of the analogue front-end was also assessed in simulation. In figure 10, a delay of about 280 ns is observed in the frequency range of interest (from low frequency up to about 300 kHz). Around 1 MHz the poles of the analogue front-end, (figure 9 blue curve), cause a sudden change in the phase which translates into the peak in the group delay graph. However, also the contributions of (i) the upstream high-voltage divider, (ii) the *ADC*, and (iii) digital filtering should be taken into account. In table 2, all these delay contributions are summarized.

If the bandwidth of the high-voltage divider is less than 1 MHz, the analogue anti-aliasing filter will be re-tuned to increase the bandwidth of the analogue front-end. In fact, as mentioned in section 3.3, a high-voltage divider is already the first stage of the considered anti-aliasing filter, thus its delay/attenuation budget has to be included into the design. In this case, the *rms* noise of the analogue front-end is not expected to increase drastically, owing to the very low-noise design. Furthermore, the delay of the digital filter can also be estimated to be about 670 ns by means of equation (3.3). Finally, the delay introduced by ADC_1 can be estimated by its datasheet to be 40 ns (on the contrary ADC_2 is not on the real-time path). In table 2, the delay contributions of the whole measurement chain is summarized.

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5.3 Worst-case repeatability

The expected WCR was assessed as defined in equation (3.4). The quantization noise of both ADC_1 and ADC_2 (assumed as purely additive) was simulated according to their $SINAD$ specifications (section 2) by means of the Pspice function RND, which generates random numbers with uniform distribution. A $10\,V_{DC}$ stimulus is given as input to the analogue front-end and the simulated quantization noise of the two $ADCs$ is added to the front-end's output in order to model the digitization of the 10 V input. The simulation is then repeated 31 times and each pair of consecutive acquisitions is used to calculate the WCR as the maximum observed value of PPR according to equations (2.1) and (3.4). In figure 11, a statistical sample of WCR ($31 - 1 = 30$ observations) is highlighted. In conclusion, the WCR assessed in simulation is lower than the superior bound of 15.4 ppm predicted from theoretical calculations in section 4.3.

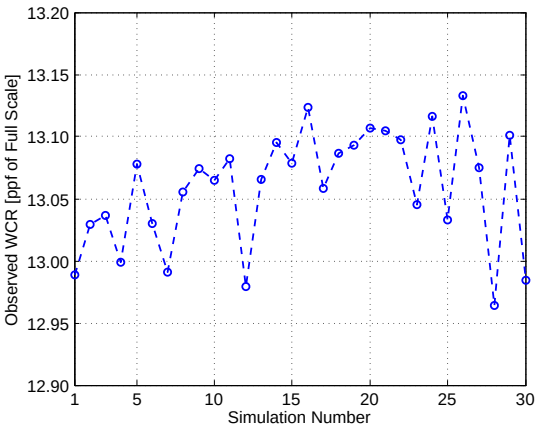

Figure 11. Observed worst-case repeatability.

6 Experimental results

In this section, the design performance assessed in simulation are verified experimentally on a prototype of the on-line digitizer developed at $CERN$.

The experimental tests assessing the performance of both the custom analogue front-end and the two $ADCs$ are reported. For the two $ADCs$, their commercially-available evaluation boards were used ($EVAL - AD7625FMCZ$ and $EVAL - AD7634EDZ$). In particular, the results of the following tests are illustrated:

- *Noise test*: the analogue noise is assessed together with the quantization noise of the two $ADCs$;
- *Bandwidth test*: the amplitude Bode diagram of the analogue front-end is measured thanks to a custom test setup in order to verify that no significant resonances are present and bandwidth requirements are met;
- *Delay test*: the group delay assessed in simulation is compared with the measured step response of the analogue front-end;

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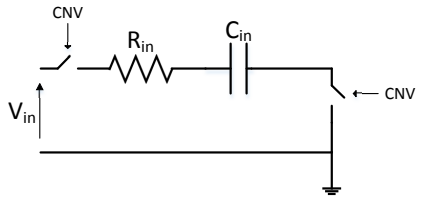

Figure 12. Equivalent circuit of the sample-and-hold input stage of the AD7625 and AD7634.

- *DC CMRR test*: the DC CMRR is assessed by means of a custom setup according to the working principle of the analogue front-end (zero-translation);
- *AC CMRR test*: the differential sensing circuit, described in section 4, allows the common-mode voltage between the high-voltage divider ground and the analogue front-end ground to be rejected. The effectiveness of this rejection is tested over a wide frequency range;
- *Full signal acquisition and Pulse-to-Pulse repeatability test*: the Pulse-to-Pulse Repeatability (PPR) of the whole on-line digitizer is measured to verify that the requirements on the main quality figure of the specific $CLIC$ application are met.

6.1 The ADCs sample-and-hold

The sample-and-hold circuits of the two $SAR\ ADCs$ exploit a capacitor C_{in} of few tens of pF (figure 12). When the pulse conversion start (CNV) arrives, the capacitor is disconnected from the input voltage source V_{in} in order to hold its voltage as constant as possible during the quantization. This switched capacitor produces a dynamic variation of the load for the upstream driving operational amplifiers, risking to generate relevant glitches. Therefore, the dynamic response of the amplifiers to the load variation is crucial in order for the voltage across the capacitor to settle within the acquisition time. If on one hand this is not a challenging problem for ADC_2, which has to sample at 600 kS/s (the driving opamp $ADA4898$ comfortably settles within the acquisition time of 310 ns), on the other hand, ADC_1 has only 40 ns of acquisition time, thus the input capacitor should be settled within this time interval.

The output amplifier $THS4531$ of the front-end is connected to the input stage of the ADC evaluation board $EVAL-AD7625FMCZ$ equipped with fast unity gain buffers (model $ADA4899$). Indeed they assure suitable bandwidth and output current to settle the capacitor within the required time for the metrological tests discussed in sections 6.6 and 6.7.

6.2 Noise test

In section 5.3, it was simulated that a WCR better than 15.4 ppm could be achieved provided that the analogue noise is lower than the quantization noise of the two $ADCs$. In this section, this assumption on the rms noise level of the analogue front-end is validated experimentally.

In figure 13(a), the setup used for the test is depicted. The trigger signal is set to 0 and the switch S_1 in figure 8 is positioned such that the difference stage (green in figure 8) subtracts the signal on the terminal x (shorted to ground in this test) from itself in order to achieve a null output $ideally$. In this case, on the differential output ($OUTp - OUTn$), only the intrinsic noise of the analogue front-end

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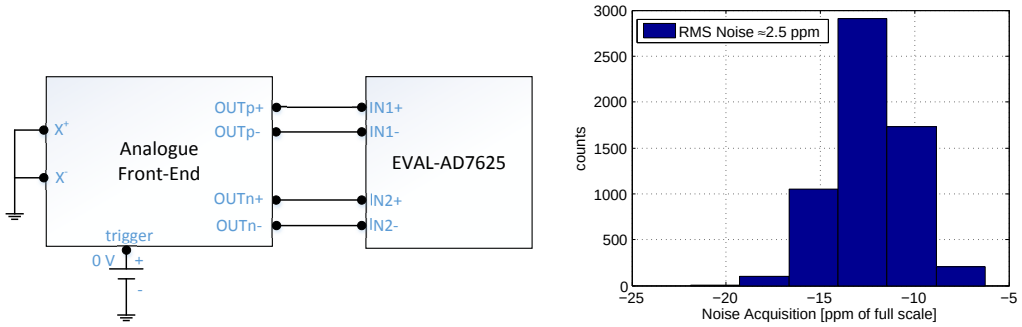
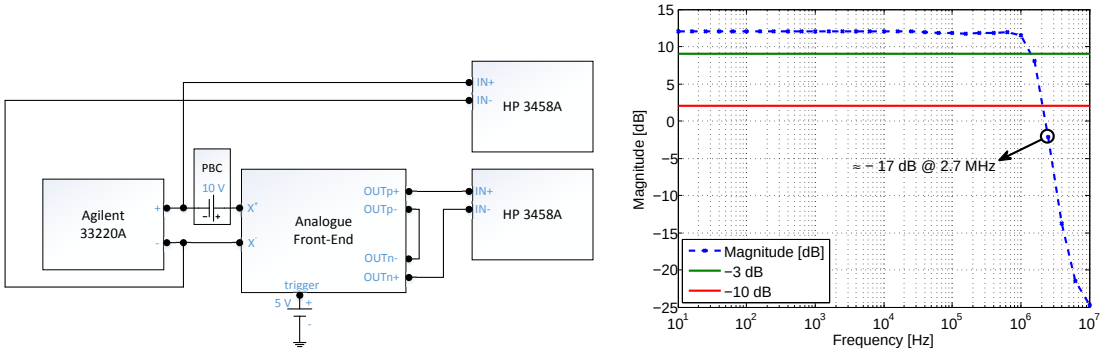


(a) Test setup for noise measurement

(b) Noise histogram

Figure 13. Noise test.



(a) Test setup for bandwidth measurement

(b) Analogue front-end's bandwidth

Figure 14. Test of analogue front-end's bandwidth.

is measured by the evaluation board of the *AD*7625. By acquiring 6.000 samples at 3 MS/s, a noise record of 2 ms is obtained. The rms noise $\sigma_{n'_{\mathrm{FE}}+n'_1} \approx 2.5$ ppm, includes the contribution of the analogue front-end and the quantization noise of ADC_1 both at 3 MS/s. The attenuation produced by the digital filter brings this value to $\sigma_{\overline{n}'_{\mathrm{FE}}+\overline{n}'_1} \approx 1.1$ ppm, thus $\sigma_{\overline{n}'_{\mathrm{FE}}} = \sqrt{\sigma^2_{\overline{n}'_{\mathrm{FE}}+\overline{n}'_1} - \sigma^2_{\overline{n}'_1}} \approx 0.6$ ppm ($\sigma_{\overline{n}'_1}$ was calculated from equation (3.6) in the specific case of the case study detailed in section 4.3). In conclusion, $\sigma_{\overline{n}'_{\mathrm{FE}}} \ll \sigma_{n_2}$ as needed from system requirements.

6.3 Bandwidth

In this test, the amplitude of the frequency response of the analogue front-end is measured in order to verify the attenuation level at $f_{AF} = 2.7$ MHz and to locate the −3 dB point. It is worth noting that in this test, only the bandwidth of the analogue front-end is measured. Given the working principle of the whole digitizer (oversampling and digital filtering) the overall bandwidth will be limited by the digital filtering as discussed in section 3.3

The experimental test setup is sketched in figure 14(a). An arbitrary waveform generator (Agilent/Keysight 33220*A*) generates a set of sine waves of 2 V_{pp}, with frequency ranging from 10 Hz to 10 MHz. The sine waves are sent both to a digital multimeter ($HP - 3458A$) and to the negative terminal of a reference *DC* voltage generator [26] (*PBC*). The positive terminal of the

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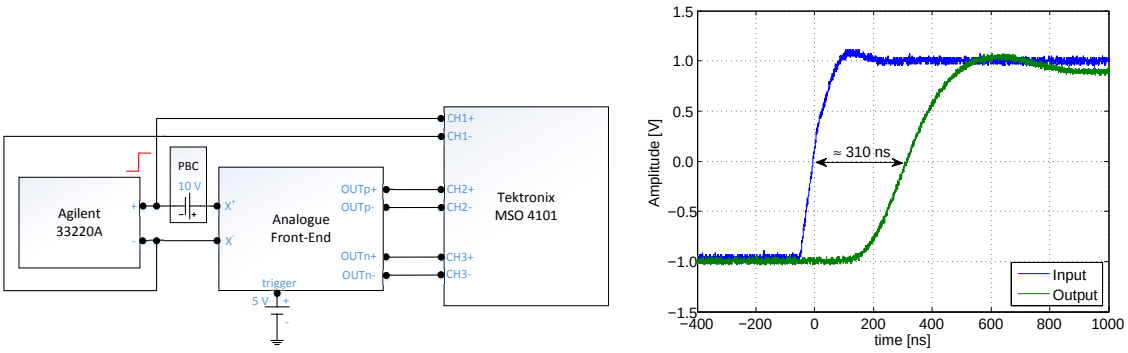

(a) Test setup for delay measurement

(b) Analogue front-end's delay (Input = CH1, Output = CH2 - CH3)

Figure 15. Test of analogue front-end's delay.

PBC applies the sine waves, shifted-up of $10\,\mathrm{V}_{DC}$, to the signal input of the analogue front-end. The DC voltage shift is needed to center the ± 1 V sine waves around 10 V in order to not activate the clipping circuitry (which clips voltages below $V_{\mathrm{clip}-} \approx 9$ V and above $V_{\mathrm{clip}+} \approx 11$ V). At this point, according to the working principle of the front-end, the $V_{\mathrm{REF}} = 10\,\mathrm{V}_{DC}$ is subtracted from the input signal and the difference is amplified by a total gain of about 4 V/V. The sine waves out of the analogue front-end are finally measured by another digital multimeter. At each step, the *rms* values of the two signals (input and output of the analogue front-end) are measured by the two multimeters ($HP-3458A$) in AC voltage mode in order to obtain the corresponding point of the Bode diagram.

The experimental results (figure 14) are compatible with the simulation outcomes of figure 9. Furthermore, an attenuation of about 17 dB is achieved at $f_{AF} = 2.7$ MHz, more than the design expectations.

6.4 Delay

In this test, the step response of the analogue front-end is measured and compared with the group delay assessed in simulation.

The test setup is shown in figure 15(a). The arbitrary waveform generator provides a step of ± 1 V, with 50 ns of rise time, to the channel 1 ($CH1$) of a digital oscilloscope. In nominal working conditions, however, such sharp transition signals are not to be expected. This test evaluates therefore a worst-case delay with respect to the simulation. Also in this case, a generator PBC shifts-up the step around 10 V in order to center it in the "non-clipping" range of the analogue front-end. The oscilloscope digitizes also the positive and negative outputs of the front-end on channels 2 and 3, respectively. In this way, by subtracting the $CH3$ from $CH2$, the results in figure 15 are obtained. A delay at 50 % of the transition of about 310 ns is observed; this value is compatible with the simulated group delay of figure 10.

6.5 CMRR

Two different test setups were used in order to characterize the $CMRR$ of the digitizer both in DC and AC.

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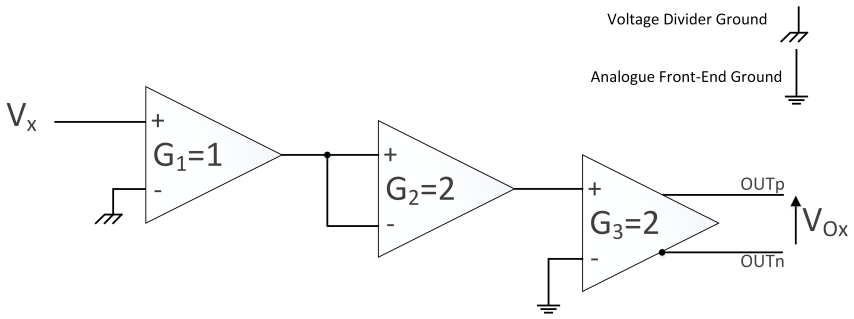
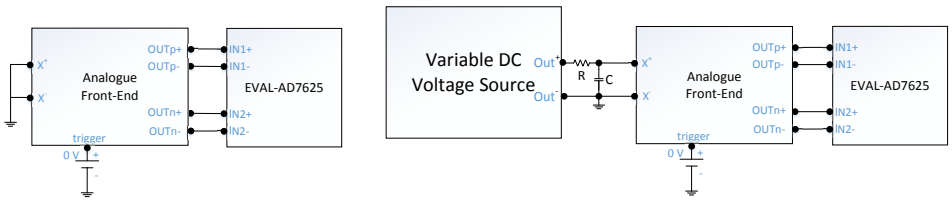


Figure 16. Configuration of the three differential stages during DC CMRR measurement.



(a) First phase (short-circuit) (b) Second phase (common-mode voltage)

Figure 17. Test setups for DC CMRR measurement.

6.5.1 DC CMRR

Given the working principle of the analogue front-end (V_{REF} subtraction first, and amplification afterwards), the Common-Mode Rejection Ratio ($CMRR$) in DC is a critical parameter. As a matter of fact, a poor $DC\ CMRR$ would have the effect of not properly center the nominal 10 V_{DC} around zero. In addition, the tolerances of the gain-setting resistors of a differential stage as in section 4 affect directly $DC\ CMRR$ performance of the stage itself [27]. For this reason, in this design, the resistor networks Vishay MPM with 0.05 % of relative tolerance were used.

It is worth noting that the definition and procedure used for this test are significantly adapted to the specific $CLIC$ application. In particular, the three differential stages of the analogue front-end were setup as depicted in figure 16. The stage responsible of rejecting the DC common mode voltage is the second difference amplifier, corresponding to the first amplifier in the green block in figure 8. By setting the switch S_1 in the appropriate position, this stage sees a common mode voltage of V_X and the level of this rejection is assessed with this test.

To do that, the $DC\ CMRR$ was measured in twofold test phases, by means of the two corresponding setups in figures 17. The $ADC\ AD7625$, controlled by its evaluation board, acquires 50 records of the front-end's offset. Each record is composed by 450 samples acquired at 3 MS/s (150 μs), emulating the acquisition of the charger voltage during the region $Pulse$ (figure 2).

- The first phase (setup in figure 17(a)) consisted of measuring the output offset of the front-end when the signal input is shorted to ground. An offset of about $V_{Osc} \approx -380\,\mu$V is measured for an input common mode voltage of $V_0 = 0$ V (shorted and grounded inputs).
- The second phase (setup in figure 17(b)) consisted of measuring the output offsets ($V_{Ox} = V_{O2} \cdots V_{O10}$) corresponding to particular input common-mode voltages. A variable DC

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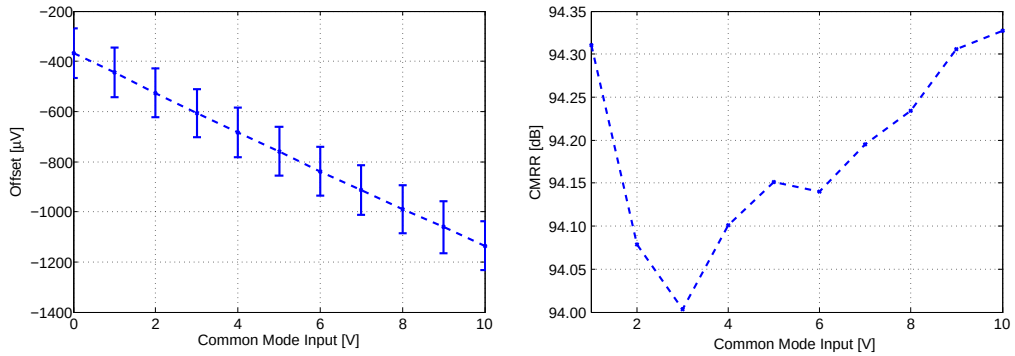
voltage source was used for generating a DC voltage $V_x = 2 \cdots 10\,\mathrm{V}$ (2 V steps), applied to the signal input of the analogue front-end. The focus was on the *DC CMRR* of the difference stage (green part in figure 8). Therefore, a first order *RC* low-pass filter ($R = 820\,\mathrm{k\Omega}$, $C = 10\,\mathrm{nF}$) was used to effectively attenuate disturbances arising from the *DC* voltage source with frequency content above 20 Hz. At each step, a common-mode voltage equal to the output of the variable DC source was applied to the circuit.

In figure 18(a), the results of 50 repeated measurements are depicted with the relative $1 - \sigma$ repeatability bands.

The Common-Mode Rejection Ratio is computed as:

$$CMRR_{\mathrm{diff}} = 20 \cdot \mathrm{Log}_{10}\left(\frac{G \cdot V_x}{|V_{Ox} - V_{Osc}|}\right) \tag{6.1}$$

where G is the gain of the front-end ($G = 4\,\mathrm{V/V}$), V_x the corresponding common-mode input, V_{Ox} and V_{Osc} the offset measured when x V are applied to the inputs and when both the inputs are shorted to ground (first phase), respectively.



(a) Output offset V_{Ox} vs common-mode input voltage V_x

(b) CMRR vs common-mode input voltage

Figure 18. Output offset and CMRR vs common-mode input voltage.

In figure 18(b), the *DC CMRR* is reported with respect to the applied common-mode input voltage. A considerable result of more than 94 dB in nominal working conditions ($V_x = 10\,\mathrm{V}$) is highlighted.

6.5.2 AC CMRR

The input stage of the analogue front-end is based on a differential sensing circuit (in violet in figure 8) [20], in order to reject the common-mode voltage between the ground of the voltage divider and the ground of the analogue front-end (figure 19).

The test setup of figure 20a, already used in [24], allows $CMRR_{\mathrm{ref}}$ to be assessed over a frequency range of 1 MHz. In this test, the *AC* common-mode voltage was imposed between the references of two *DC* generators. A Transfer Function Analyzer (*TFA* also known as Frequency Response Analyzer or Gain Phase Analyzer) Powertek *GP* 102 was used to generate a set of sine waves (2 V amplitude), ranging in frequency from 10 mHz to 1 MHz. The sine waves were applied

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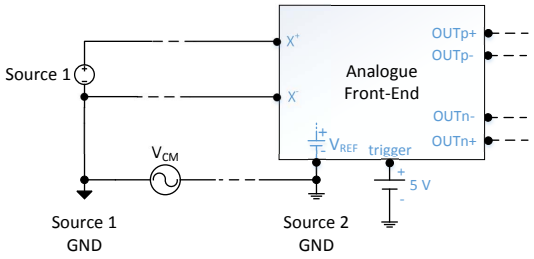
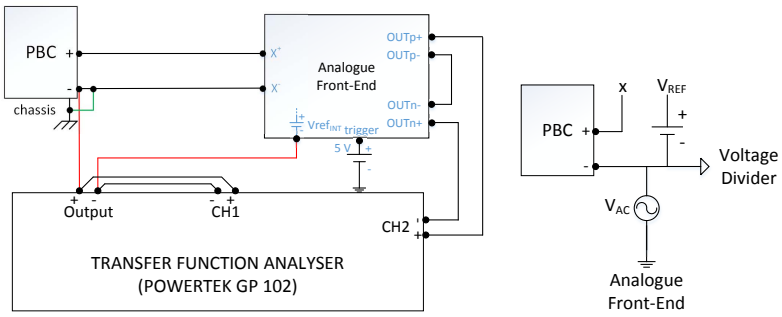


Figure 19. The effect of two far grounds [28].

between the chassis reference of a fully floating DC 10 V portable generator (PBC) [26], and the local ground of the analogue front-end. The PBC, in turn, fed the signal input of the front-end by fixing the static working point at 10 V. Amplitude and phase (difference) of the input sine waves and the output of the front-end were then measured by the TFA in order to determine the Bode diagram.



(a) $CMRR_{\text{ref}}$ measurement setup (b) V_{CM} definition

Figure 20. Test setup for $CMRR_{\text{ref}}$ measurement and V_{CM} definition.

In this test, the PBC emulates the signal from the voltage divider, whereas the input V_{REF} is connected to the 10 V_{DC} reference voltage (V_{REF}) by means of the switch S_1. The configuration of the test setup in figure 20a highlights how the chassis of the PBC is connected to the negative terminal of the differential signal input x on the front-end (not connected to the local ground). Conversely, the reference voltage of V_{REF} is directly connected to the front-end's ground. Figure 20b shows how V_{AC} is combined at the input stage and highlights the common mode voltage actually experienced by the front-end:

$$V_{CM} = \frac{x + V_{\text{REF}}}{2} = \frac{(V_{PBC1} + V_{AC}) + V_{\text{REF}}}{2} = 10\,V + \frac{V_{AC}}{2} \tag{6.2}$$

The DC part of V_{CM} (10 V) is rejected as explained in section 6.5.1, while the measurement of the rejection of $V_{AC}/2$ is the actual purpose of this test. Analogously as the $CMRR_{\text{diff}}$ in (6.1),

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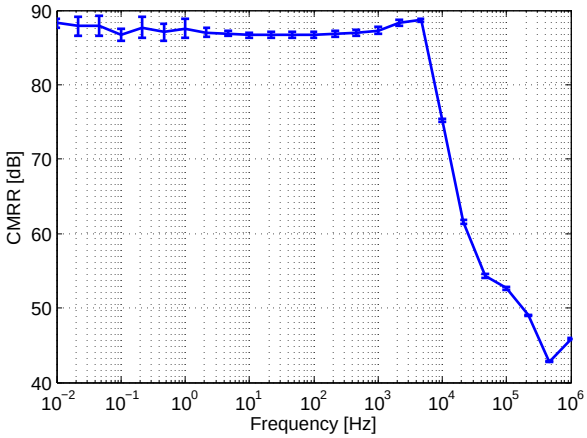

Figure 21. *CMRR* of the circuit for rejecting common mode voltage between the voltage divider and the local ground (*1-σ* repeatability bands).

$CMRR_{\text{ref}}$ can be defined as:

$$\begin{aligned} CMRR_{\text{ref}} &= 20 \cdot \text{Log}_{10}\left(\frac{G_D}{G_{CM}}\right) = 20 \cdot \text{Log}_{10}\left(\frac{G_D V_{CM}}{V_{\text{out}}}\right) = \\ &= 20 \cdot \text{Log}_{10}\left(\frac{G_D V_{AC}}{2 \cdot V_{\text{out}}}\right) \\ &= 20 \cdot \text{Log}_{10}\left(\frac{G_D V_{AC}}{V_{\text{out}}}\right) - 20 \cdot \text{Log}_{10}(2) \end{aligned} \tag{6.3}$$

where G_D and G_{CM} are the differential and common-mode gains, respectively, and V_{out} is the voltage output of the analogue front-end. This shows that a correction factor of $-20 \cdot \text{Log}_{10}(2)$ needs to be applied to the instrument reading.

The average results obtained over 10 repetitions with the *1-σ* repeatability bands are shown in figure 21. The $CMRR_{\text{ref}}$ of about 87 dB up to 5 kHz decreases at higher frequencies down to about 45 dB at 1 MHz which is still a considerable result.

6.6 Full signal acquisition and pulse-to-pulse repeatability

The test setup in figure 22(a) allows the full reconstruction of a 10 V signal to be verified and the experimental Pulse-to-Pulse Repeatability (*PPR*) of the whole on-line digitizer to be assessed. The floating generator *PBC* [26] emulates the voltage of the voltage divider by providing a 10 V signal at the input of the analogue front-end. The nominal working conditions are emulated by shorting the negative terminal of the *PBC* to a fixed potential, different from the front-end's ground. The *ADC AD*7625, controlled by its commercial evaluation board, digitizes at 3 MS/s the input signal conditioned according to the working principle of the front-end. At the same time, the *ADC AD*7634, by its evaluation board, acquires at 600 kS/s the internal reference voltage (V_{REF}), which is subtracted from the input signal in order to be centered around zero. In post-processing, the signal coming from the *AD*7625 is filtered and decimated as discussed in section 3.3, in order to reduce the final throughput to 600 kS/s. Furthermore, offset and gain compensations for the analogue front-end were applied according to equation (3.2).

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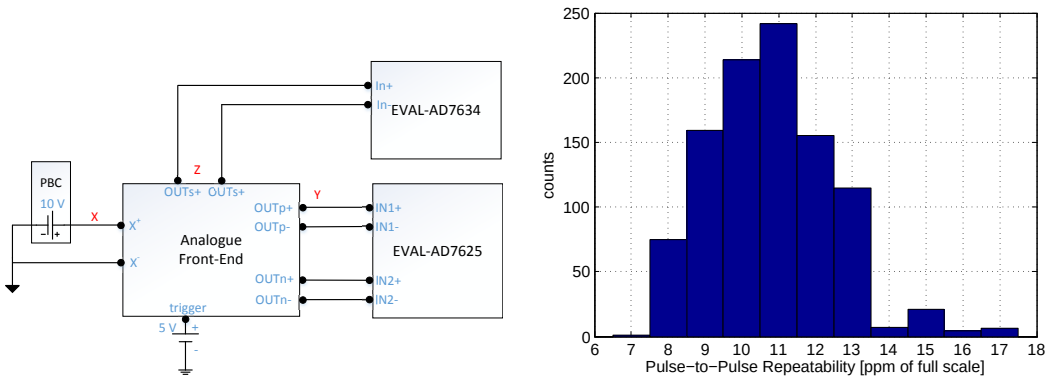

(a) Test setup for full signal reconstruction and PPR measurement

(b) Pulse-to-Pulse Repeatability in nominal working conditions

Figure 22. Pulse-to-pulse repeatability measurement.

The post-processing operations for reconstructing the original signal are:

$$X_k = Z_k + \frac{1}{N \cdot G^m} \sum_{i=1}^{N} (Y_i - Ox^m) \tag{6.4}$$

The subscript k refers to data delivered at 600 kS/s; the variable Y_i needs to be averaged and decimated by a factor $N = 5$ in order to be combined with Z_k. G^m is the overall gain of the analogue front-end obtained as the average of the first 10 points of figure 14. Ox^m is the offset of the front-end when working in nominal working conditions.

For PPR measurement, the analogue front-end input was connected to a 10 V source (PBC) and the corresponding offset was measured by a digital multimeter (model $HP - 3458A$). In this configuration, the measured offset is given by the difference between the input 10 V (PBC) and the internal reference ($LT1236$), amplified by the front-end's gain (neglecting the effect of non-infinite $DC\ CMRR$). Thus, the variable X_k was measured 1000 times (each acquisition lasts 150 μs, as in nominal working conditions) and the PPR definition of equation (2.1) was applied in order to obtain the histogram depicted in figure 22(b). The mode of the experimental PPR is clearly lower than 15.4 ppm and shows a good agreement with theoretical prediction and simulation results achieving the main design goal of the $CLIC$ application.

6.7 Accuracy

Though the $CLIC$ application requirements only concern repeatability (in particular Pulse-to-Pulse Repeatability as defined in equation (2.1)), for the sake of completeness, the accuracy of the proposed on-line digitizer was also assessed in this work. Clearly, the proposed digitizer must be firstly calibrated in order to compensate gain and offset errors both of the analogue front-end and the two $ADCs$. Two calibration strategies are proposed according to the accuracy requirements of the specific application.

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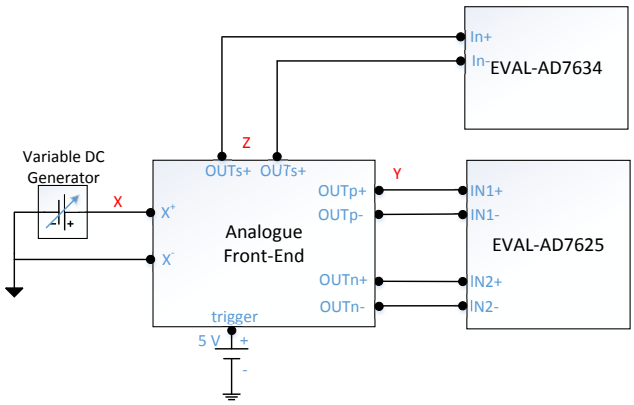

Figure 23. Test setup for accuracy error assessment.

6.7.1 Coarse calibration

The first procedure consists on a single-step, two-points calibration; by shorting the input x to ground and acquiring the voltages on the two $ADCs$, the offset error can be estimated. Afterwards, to assess the gain error, a variable DC generator was connected both to the input of the instrument and to a digital multimeter ($HP-3458A$). By firstly compensating the offset, the remaining error (obtained as the difference between readings of the instrument and the $HP-3458A$) was modeled as a gain error. In conclusion, by this procedure, two global calibration constants are required, the gain and offset errors.

6.7.2 Fine calibration

The second procedure allows higher accuracy by means of a two-step, two-point calibration. The first step consists in compensating the gain and offset errors of the analogue front-end, computed as in section 6.6. Afterwards, the procedure described in 6.7.1 is executed in order to assess the gain and offset errors of the combination of the two $ADCs$. Thus, in this case, four calibration constants are required, gain/offset errors of the front-end (first step) and gain/offset errors of the $ADCs$ (second step).

6.7.3 Results

The two calibration procedures were applied to the proposed instrument and the relative accuracy error was assessed by means of the test setup of figure 23. At each step, a variable DC generator sends to the analogue front-end a DC voltage ranging from 9 V to 11 V (0.5 V steps) and the corresponding output is measured by the two $ADCs$. After applying the two compensation procedures, the accuracy error can be assessed by comparing the reading of the proposed instrument to the one obtained with the digital multimeter $HP-3458A$. Figures 24, show the accuracy errors obtained with the two calibration procedures. Obviously, the fine calibration allows a more effective reduction of the reconstruction error.

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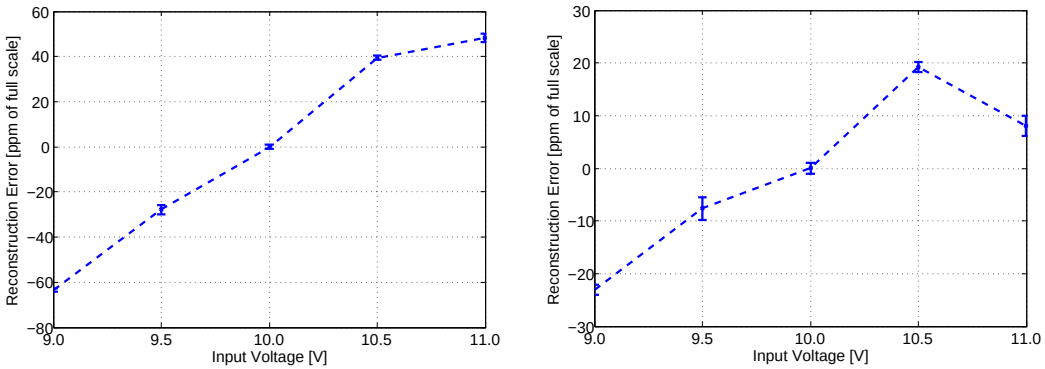

(a) Coarse calibration

(b) Fine calibration

Figure 24. On-line digitizer error distribution.

7 Conclusion

The proof of principle of a custom on-line digitizer for controlling the high-voltage of power converters has been presented. Starting from the requirements, the concept design and a physical architecture are presented and discussed.

Pspice simulations were performed to demonstrate the effectiveness of the proposed architecture with respect to the defined requirements in a very challenging case study of the *CLIC* accelerator under study at *CERN*. Experimental test setups allowed the performance of the prototype developed at *CERN* to be assessed, by highlighting also compatibility with the design simulation results.

In conclusion, noise, bandwidth, *DC CMRR* and Pulse-to-Pulse Repeatability (*PPR*) were demonstrated to be comfortably inside the requirements of the case study, while the delay turned out to be very critical at the required bandwidth, even if still inside the specification.

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