Partial Power Processing using a Flyback converter: design and comparison

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***Abstract*—PPP (Partial Power Processing) involves designing a converter that splits the processed power between two converters: one with a fixed conversion ratio and high efficiency, and the other with a variable conversion ratio and lower efficiency. Although the potential of this class of converter can be highly effective, it is not suitable for all applications. Literature lacks consistent terminology and clear definitions of which converter topologies perform true PPP. Some papers analyze the PPP as a general concept, others comparing specific conversion topologies. This paper aims to test a flyback converter prototype in the two layouts, explaining efficiency variations through advanced modeling and design methods.**
As expected, the partial power converter outperforms the full power converter. Performance is evaluated in terms of semiconductor component stress, snubber circuit impact, and overall efficiency.

***Index Terms*—Partial Power processing, Flyback converter, Conversion efficiency, Converter's design, Converter's sizing, Converter's modeling**

I. Introduction

Literature on Partial Power Processing (PPP) covers various aspects. Paper [1] is a very comprehensive review of the PPP (Partial-Power Processing) concept and its implementation, introducing three main PPP converter families: PP (Partial Power) converters, DP (Differential Power) converters, and FP (Fractional Power) converters. It highlights the IPOS (Input parallel Output series) configuration and the ISOP (Input series Output parallel) configuration and outlines the main drawbacks of PPP: No PPP architecture ensures galvanic isolation between the source and the load; Low voltage elements inside the converter necessitate an over-voltage protection circuit during startup; In PPCs, the processed power ratio depends on the static voltage gain, making them inadequate for high step-up/down applications.

Paper [2] explores the efficiency and power density of partial active power converters compared to full active power converters, emphasizing that performance depends on both active and nonactive power within the converter. It introduces the term PAPP (Partial Active Power Processing) for converters where PPP benefits apply only to active power.

Paper [3] proposes an analytical method to evaluate power processed by PPP converters, distinguishing true PPP topologies from partial active power processing topologies. It demonstrates that some series regulator topologies may not reduce nonactive processed power, analyzing FBPS (Full Bridge Phase Shift) and flyback converters in IPOS configurations without detailed modeling or design process discussion.

Paper [4] defines the component stress factor as the ratio between apparent power and active power, comparing FBPS and FB/PP (Full-bridge/Push–pull) topologies.

Paper [5] reviews nearly 30 papers on unidirectional and bidirectional IPOS and ISOP PP converters for DC/DC applications, proposing considerations for active and nonactive power in various topologies. It introduces power processing and Fryze power factors for evaluating converters and demonstrates optimizing the turns ratio of magnetic devices to reduce nonactive power and improve converter Fryze PF, ensuring PPP.

Paper [6] reports the basic equations of conversion gain of several converters in full power and partial power configuration. The proposed structures are flyback converter, forward converter, isolated Cuk converter, isolated Sepic converter, isolated Zeta converter. Paper [7] presents a high step-up SEPIC-based partial-power converter. The flyback IPOS PP circuit and the modified SEPIC circuit are connected in cascade therefore the two voltage gains are multiplied, obtaining high voltage gain without extremely high duty cycle over a wide input range. As for this two-stage converter, the first stage is the partial-power Flyback which is responsible for regulating the voltage within the wide input range and the second stage operates in a fixed state while providing zero-voltage soft switching.

Paper [8] analyzes a flyback converter in IPOS PP, ISOP PP, and full power configurations, providing a prototype to verify results. Inspired by [8] and it propose almost the same conversion structure using the flyback converter. In addition to [8], this paper proposes a similar conversion structure using a flyback converter, aiming to explain increased PPP efficiency through modeling and design. The proposed modeling results in a switched state-space model including

extended modeling of the transformer, source, and snubber circuit. The design method sets requirements for continuous or discontinuous conduction mode operation, validated by a prototype tested in Full Power Processing (FPP) and PPP layouts. The results discuss semiconductor component stress, snubber circuit impact, and efficiency variation.

Paper [9] collects the analytical expressions of voltage gain, conversion efficiency and bidirectional power flow features of the general IPOS and ISOP PP DC/DC converters. The information, derived from the previous analysis, is used to design a flyback IPOS PP. It has two MOSFET, instead of the diodes, on the two sides of the HF transformer. The PP converter is used to implement a BESS charger. The modeling is based on a simplified version of a flyback that does not consider recovery diodes and snubber circuits. One of the quantities that much affects the design of PP flyback converter is the turns ratio of the transformer. If the turn ratio is close to 1 the converter may offer higher efficiency with lower currents. With lower turn ratios, the efficiency decreases due to the higher currents in the primary or secondary transformer windings. In case of high turn ratios, the voltage stress on components is very high, reducing the advantages of PPP concept.

The IPOS PP flyback converter for a BESS application is also presented in [10]. In this paper, the converter is not used as battery charger, there are distributed converters configuration implementing balancing functionality and power stage regulation functionality into one system. The term "partial power converter" is not properly used, because the presented conversion system is a "differential power converter".

Paper [11] deals with a ISOP PP flyback converter for the solar PV system. Some sizing equations are provided to describe the design of the transformer and the capacitive output filter. The simulation outcomes result in highlighting the increasing of efficiency in PPP configuration compared to full power configuration. This increasing of efficiency depends on the little input/output voltage ratio of the converter and, in general, on the proper selection of the operating range. In other papers, as [3] and [8], the ISOP PP flyback converter is put aside because its range to perform PPP is very restricted.

II. Modeling and sizing

To describe the proposed sizing method, two mathematical electrical models of the flyback converter are presented. The first model, with ideal components, sets sizing criteria. The second model includes components like the flyback diode and snubber circuit to describe effective operation. The load is an equivalent Thevenin circuit, representing a battery or other load. State space equations use V_b and V_in as input.

A. Basic modeling

The operating principle of the flyback converter is reported using its basic mathematical model. The electric structure is depicted in Fig. 1.

In CCM (Continous Conduction Mode), the converter switches between two configurations (with T_s as the switching period and D as the duty ratio): - during DT_s, the switching device is closed and the diode is not conducting current; - during $(1-D)T_s$, the switching device is open and the diode is conducting current. In case of DCM (Discontinuous Conduction Mode), there is a time interval with no current flow. The current flows in the switching device for DT_s, the time interval in which the diode is forwarded depends on the sizing of the converter. When the diode starts conducting, the current is decreasing and it is zeroed before the end of the switching period. When the current in the diode become zero, both the transformer's primary and secondary voltages tends to zero and the converter remains un-supplied until the end of switching period.

The CCM and DCM can occur in the converter varying the duty ratio, or the same duty ratio can result in the two conduction modes based on the sizing of the converter.

The equation of the three configurations of the system are reported:

$\boxed{u_1 = 1; \quad u_2 = 0}$

$$\begin{aligned} di_p/dt &= V_{in}/L_p \\ di_s/dt &= 0 \\ dv_C/dt &= (V_b - v_C)/CR_b \\ v_p &= V_{in} \\ v_s &= L_m V_{in}/L_p \\ i_{in} &= i_p \\ i_{out} &= (v_C - V_b)/R_b \end{aligned} \tag{1}$$

$\boxed{u_1 = 0; \quad u_2 = 1}$

$$\begin{aligned} di_p/dt &= 0 \\ di_s/dt &= -v_C/L_s \\ dv_C/dt &= (V_b - R_b i_s - v_C)/CR_b \\ v_p &= -(L_m v_C)/L_s \\ v_s &= -v_C \\ i_{in} &= i_p \\ i_{out} &= (v_C - V_b)/R_b \end{aligned} \tag{2}$$

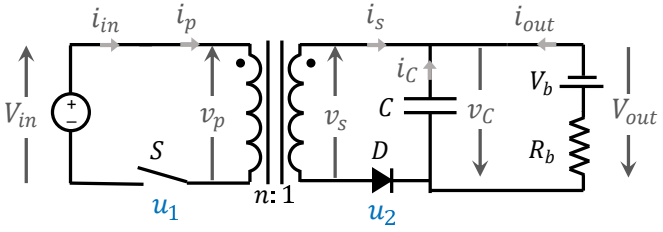

Fig. 1. Basic equivalent electrical model of the full power flyback converter.

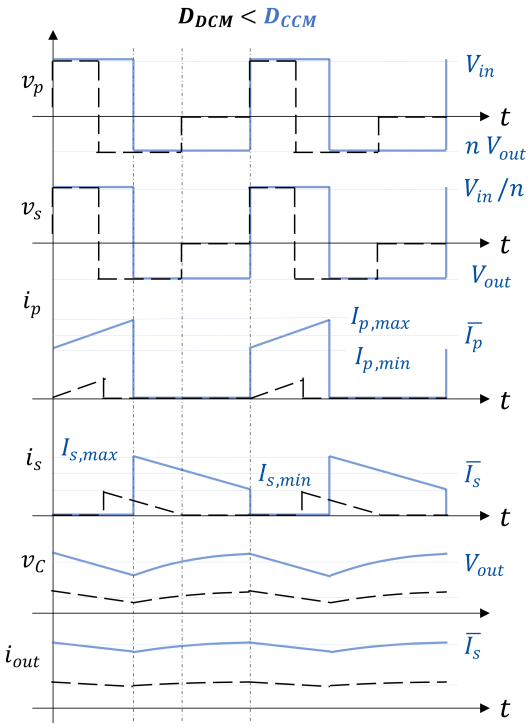

Fig. 2. Operating behaviour of the basic model of flyback converter in CCM and DCM.

$\boxed{u_1 = 0; \quad u_2 = 0}$

$$\begin{aligned} di_p/dt &= 0 \\ di_s/dt &= 0 \\ dv_C/dt &= (V_b - v_C)/CR_b \\ v_p &= 0 \\ v_s &= 0 \\ i_{in} &= 0 \\ i_{out} &= (v_C - V_b)/R_b \end{aligned} \tag{3}$$

The output current limit between CCM and DCM is determined by combining the equations (1)-(3).

$$I_{out,lim} = V_{in} n D(1-D)/2 f_s L_p \tag{4}$$

If the output current is higher that value, the operating mode is CCM; it is DCM otherwise. The two modes the following equations can be obtained:

CCM - $\boxed{I_{out} > I_{out,lim}}$

$$\begin{aligned} V_{out}/V_{in} &= D/n(1-D) \\ \Delta I_p &= V_{in} D/L_p f_s \\ \Delta I_s &= n\Delta I_p = V_{out}(1-D)/L_s f_s \end{aligned} \tag{5}$$

DCM - $\boxed{I_{out} < I_{out,lim}}$

$$\begin{aligned} V_{out}/V_{in} &= V_{in} D^2/2 f_s L_p I_{out} \\ \Delta I_p &= V_{in} D/L_p f_s \\ \Delta I_s &= n\Delta I_p \end{aligned} \tag{6}$$

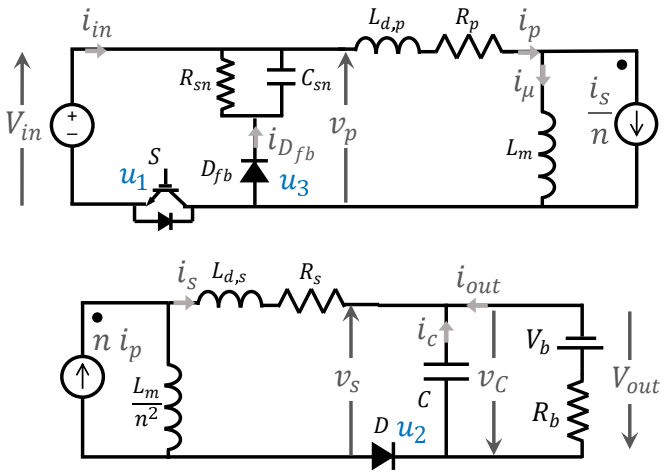

Fig. 3. Improved equivalent electrical model of the full power flyback converter.

Fig. 2 shows the operating behaviour of the flyback converter in both modes, with the solid blue line representing CCM and the dashed line representing DCM. The same model yields both modes using different duty ratios.

B. Improved modeling

The basic model is useful to understand the working principle, but it is not adequate for simulation or detailed mathematical analysis. In Fig. 3, the equivalent electric circuit of the converter includes the flyback diode, D_{fb}, which gives its name, and models the HF transformer with an equivalent T-model. In this model, L_m represents the magnetizing inductance, $L_{d,p}$ and $L_{d,s}$ denote the inductive losses on the primary and secondary sides, respectively, and R_p and R_s represent the Joule losses on the primary and secondary sides, respectively. The three boolean variables u_1, u_2 and u_3 are describing the conduction states of the MOSFET and the diodes: when these variables are one, the corresponding switching devices are in a short circuit state. For pagination reasons, the two sides of the transformer are split into two parts in the figure.

This modeling approach allows for the description of additional effects of the converter, as illustrated in Fig. 4. The solid blue line refers to the CCM, while the dashed line is the DCM.Both modes are derived from the same model using different duty ratios.

Unlike in Fig. 2, the currents i_p and i_s rise and fall smoothly. While i_p is decreasing, the flyback diode conducts, and the primary voltage equals that of the snubber circuit. In Fig. 4, the voltage during this period is one and a half times Vin, but this value can be reduced by adjusting the snubber components. In DCM, the snubber circuit primarily affects the off period of the converter.

Under normal operating conditions and with the correct sizing process, the sequences of u1, u2, and u3 should be as follows:

- CCM: $110 \rightarrow 100 \rightarrow 011 \rightarrow 010 \rightarrow 110$
- DCM: $000 \rightarrow 100 \rightarrow 011 \rightarrow 010 \rightarrow 000$

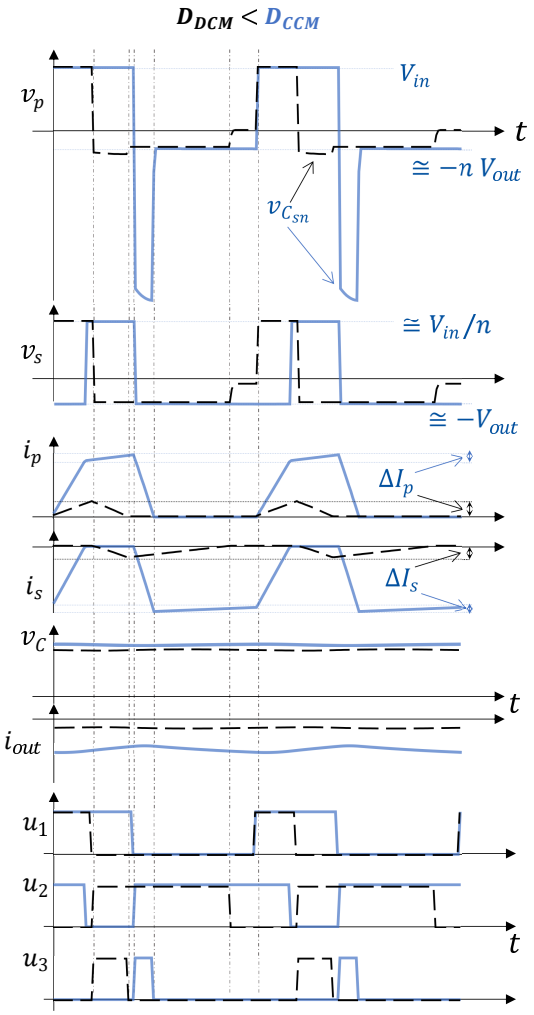

Fig. 4. Operating behaviour of the improved model of flyback converter in CCM and DCM.

C. Basic sizing

The basic sizing process starts from the definition of the requirements of the transformer, followed by determining the sizes of the semiconductor elements and filters. The common input sizing requirements include: V_{in}, f_s, the range of V_b and R_b variation, $I_{out,max}$, $\Delta I_{p,max}$, $\Delta I_{s,max}$, $\Delta V_{C,max}$ and $\Delta V_{C_{sn},max}$. Essentially, the maximum and minimum desired values of the duty ratio D need to be determined. The maximum value, D_{min}, is limited by the transformer technology and category, while the minimum value, D_{max}, depends on the desired mode of operation for the converter.
The converter can work in both CCM and DCM by varying the duty ratio, but the limit value of the output current also depends on other circuit parameters. Consequently, two different sets of equations are proposed to size the converter's transformer for the two modes. When using the sizing equations for CCM, the converter will operate in CCM from D_{min} to D_{max} and in DCM from 0 to D_{min}. If the converter is sized using the DCM set of equations, it shall operate in DCM from 0 to D_{max}. It is important to note that in a real-world converter, the operating range in CCM and DCM may be reduced due to unmodeled effects.
The output sizing parameters should inlcude: n, L_m, L_p, L_s, the target voltage $V_{MOSFET,max}$ and current $I_{MOSFET,max}$ on the MOSFET, the maximum voltage on the output diode V_D, the snubber circuit parameters R_{sn} and C_{sn} and its voltage $V_{C_{sn},max}$ and its power $P_{R_{sn},max}$.
The two sets of equations for the transformer sizing are inequalities derived from equations (5) and (6):

CCM

$$\begin{aligned} n &\geq \frac{V_{in,max} D_{min}}{V_b(1-D_{min})} \\ L_m &> \frac{V_{in,max} V_{out,max}}{f_s P_{out,min}} \\ L_m &> \frac{V_{in,max} D_{min}}{f_s \Delta I_{p,max} n} \\ L_m &> \frac{n(V_b - \sqrt{P_{out,max} R_b})}{f_s \Delta I_{s,max}} \end{aligned} \tag{7}$$

DCM

$$\begin{aligned} n &\geq \frac{V_{in,max} D_{max}}{V_b(1-D_{max})} \\ L_m &> \frac{V_{in,min}^2 * D_{max}^2}{(2 * fs * P_{out,n})} \\ L_m &> \frac{V_{in,max} D_{max}}{f_s \Delta I_{p,max}} \end{aligned} \tag{8}$$

where $V_{out,max} = V_{b,max} + R_b I_{out,max}$ and $P_{out,n} = (V_b I_{out,max} + R_b I_{out,max}^2)$.
In (7), the power $P_{out,min}$ is the minimum output power required for the converter to operate in CCM. This value cannot be set to 0, the right value could be not smaller than $10 \cdot P_{out,n}$. In the equations (7) and (8), L_m is determined as the maximum value that meets all conditions. Moreover, some formulas are applied: $max(D(1-D)) = 1/4$, $max(1-D) = 1$, $L_p = nL_m$, $L_s = L_m/n$.
In the model in Fig. 3, the core losses are not modeled, so the power losses are the only joule ones. In both operating modes, the transformer efficiency is managed by monitoring the leakage resistance:

$$\begin{aligned} R_p &< \frac{n P_{out,n}(1/\eta_{TRAFO} - 1)}{8 I_{out,max}^2} \\ R_s &\leq R_p/n^2 \end{aligned} \tag{9}$$

The maximum voltage on the MOSFET is the sum of V_{in} and v_p induced by the secondary side of the transformer; the current is the maximum value of i_p. The maximum value of voltage and current values for the MOSFET are the same of those of the flyback diode: the voltage and current increase in the MOSFET and decrease in the flyback diode starting from the same maximum points.
The maximum voltage on the snubber circuit occurs when the MOSFET is turned off and the flyback diode conducts; it depends on the voltage on the transformer's secondary side. The snubber circuit voltage reaches its maximum value when i_p is not yet zero. If the snubber resistor is too small, the

average voltage of the snubber capacitor would be significantly higher than V_{in}, complicating proper insulation. Conversely, if the snubber resistor is too large, the current i_p would not reach zero within the time interval less than $(1-D)/f_s$ resulting in the secondary side diode remaining off permanently. Although the analytical expression for $I_{R_{sn},max}$ is not provided, this value should be a small fraction of $I_{MOSFET,max}$.
Furthermore, the snubber capacitor is sized so that the time constant of the snubber circuit is ten times the switching period; this prevents the capacitor from discharging before the next switching period. The secondary side current runs through the diode, with its maximum value depending on the current stored in the transformer during the MOSFET turn-on time. The maximum voltage on the diode is the sum of the output voltage and the transformer's secondary side voltage.
Therefore, the MOSFET, the output diode, the flyback diode, and the snubber circuit should meet these requirements:
CCM

$$\begin{aligned} V_{MOSFET,max} &\geq V_{in,max} + \frac{n(1-D_{min})V_{out,max}}{D_{min}} \\ I_{MOSFET,max} &\geq \frac{I_{out,max}}{(1-D_{max})} + \frac{V_{in,max}D_{max})}{2f_sL_p} \end{aligned} \tag{10}$$

$$\begin{aligned} V_{D_{fb},max} &= V_{MOSFET,max} \\ I_{D_{fb},max} &= I_{MOSFET,max} \end{aligned} \tag{11}$$

$$\begin{aligned} V_{C_{sn},max} &\geq n(1-D_{min})V_{out,max}/D_{min} \\ I_{R_{sn},max} &\geq I_{MOSFET,max}/50 \\ R_{sn} &= V_{C_{sn},max}/I_{R_{sn},max} \\ C_{sn} &= 1/(0.1R_{sn}f_s) \end{aligned} \tag{12}$$

$$\begin{aligned} V_{D,max} &\geq V_{out,max} + V_{in,max}/n \\ I_{D,max} &\geq I_{MOSFET,max}n(1-D_{max})/D_{max} \end{aligned} \tag{13}$$

DCM

$$V_{MOSFET,max} \geq V_{in,max} + \frac{V_{in,max}^2 D_{max}^2}{fsLpI_{out,max}}$$

$$\begin{aligned} I_{MOSFET,max} &\geq V_{in,max}D_{max}/f_sL_p \\ V_{D_{fb},max} &= V_{MOSFET,max} \\ I_{D_{fb},max} &= I_{MOSFET,max} \end{aligned} \tag{14}$$

$$\begin{aligned} V_{C_{sn},max} &\geq \frac{nV_{in,max}^2 D_{max}^2}{fsLpI_{out,max}} \\ I_{R_{sn},max} &\geq I_{MOSFET,max}/50 \\ R_{sn} &= V_{C_{sn},max}/I_{R_{sn},max} \\ C_{sn} &= 1/(0.1R_{sn}f_s) \end{aligned} \tag{15}$$

$$\begin{aligned} V_{D,max} &\geq V_{out,max} + V_{in,max}/n \\ I_{D,max} &\geq V_{in,max}n/4fsLp \end{aligned} \tag{16}$$

The list of requirements in equations (7) to (16) should not be considered as optimized sizing but rather as a collection of physical constraints based on both basic and improved modeling. Using these constraints, the design does not guarantee optimal performance, but it ensures the working range is well predicted and controlled.

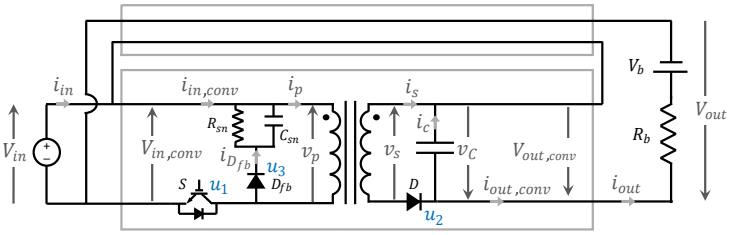

Fig. 5. Basic equivalent electrical model of the partial power flyback converter.

III. Partial Power Process (PPP)

In this section, the flyback converter is implemented in the PPP (Partial Power Processing) configuration using an Input Parallel Output Series (IPOS) layout. The main advantages of the PPP configuration include reduced converter size and device losses, leading to decreased stress on the switching devices.
The electrical equivalent scheme of the converter in this layout is depicted in Fig. 5. The two grey frames enclose the flyback converter and the direct connection between the source and the load; this connection can be seen as a dummy converter.
From the source side, both frames share the same input voltage. From the load side, their outputs are connected in series. The labels $V_{in,conv}$ and $V_{out,conv}$ regards the input and output voltages of the only flyback converter, distinct from V_{in} and V_{out}, which are the input and output voltages of the entire PP converter. In the IPOS layout, the relationship between the input and output voltages and currents is:

$$\begin{aligned} i_{out} &= i_{out,conv} = i_{in} - i_{in,conv} \\ V_{out} &= V_{out,conv} + V_{in} \\ V_{in} &= V_{in,conv} \end{aligned} \tag{17}$$

The working principle of the flyback converter in IPOS PPP remains the same as that of the full power converter described in the previous section. The PPP layout does not affect the switching sequence of u_1, u_2 and $u_3$or the operational ranges of CCM and DCM.
The previous section's models, which describe the flyback converter with an ideal voltage source as input and an equivalent Thevenin circuit as output, can be adjusted for the flyback as a partial power converter. For the IPOS PPP layout, equations (6) and (7) remain unchanged except for the substitution of V_{in} and V_{out} in $V_{in,conv}$ and $V_{out,conv}$.
The electrical quantity profiles of the converter in partial power mode are similar to those in the full power flyback converter, as shown in Fig. 4.
The design process for the FPC and PPC results in different sizes for the flyback converter due to the differing amounts of processed power and working voltages. However, by using appropriate constraints in the sizing approach, the working areas of the two converters can overlap. The flyback prototype converter discussed in the next section is designed with the constraint that the conversion system in both layouts can

provide the same output voltage from the same input source. This condition simplifies the comparison between FPC and PPC.

IV. Experimental Results

A. Sizing and expectations

The modeling and the designing methods, presented in the previous sections, are now used as guideline to build a real prototype. The sizing is based on a trade-off, so the implemented converter can be tested as both FPC and PPC in order to analyze the differences between the two layouts.
The prototype is not designed from scratch, it is the product of commercial parts assembly. One of the leg of the three-phase inverter "BOOSTXL 3PHGANINV" by Texas Instrument® has been used to realize the primary side of the converter, that means the input mosfet and the flyback diode. The transformer is a planar one by Pyton Planar®; its frequency range is suitable for the application, though the nominal power is far from that of the presented experiment. The other components are specially sized for the application.
The prototype has been used to validate the presented state-space models through numerical analysis in Matlab/Simulink® enviroment.
The Table I includes the parameters of the prototype, they are determined based on the sizing equations (5) and (10)-(13), together with the commercial and technical constraints. In order to compare the experimental results with the simulation, the Table II incorporates the transformer's model parameters derived from the identification of the transformer. The identification was implemented using methods typically used for low frequency transformers supplied with sinusoidal voltage. Some of the discrepancies between the model and the experiments could be caused by this identification method, however, more complex identification methods have not been used because they are out of the scope of this paper.
Based on the first results on the experimental prototype, the input generator is not modeled as an ideal generator in the simulation, it is modeled as in the Fig. 6 instead. It is an ideal generator with an indicator and a capacitor with their corresponding conduction losses.
In addition, the converter prototype has been obtained using the built-in flyback diode and mosfet of a commercial three phase inverter board. The power electronic board introduces parasitic effects that adds divergence between model and prototype.

TABLE I
Parameters of the flyback converter prototype

Parameter	Symbol	Value
Transformer		
Nominal power	$P_{n,nom}$	5.6 kW
Nominal voltage on primary side	$V_{p,nom}$	102 V
Nominal voltage on secondary side	$V_{s,nom}$	560 V
Transformation ratio	n	1/5.5
Nominal frequency in square wave	f_s	100 kHz
Mosfet		
Drain-to-source On-resistance	$R_{DS,mosfet}$	20 $m\Omega$
Max drain-to-source voltage	$V_{DS,mosfet}$	80 V
Max gate-to-source voltage	$V_{GS,mosfet}$	12 V
Total Gate Charge	C_{mosfet}	3.8 nF
Snubber circuit		
Diode - Forward threshold voltage	$V_{T,D_{sn}}$	0.65 V
Diode - Forward voltage drop	$V_{F,D_{sn}}$	1 V
Diode - Forward resistance	$R_{D,D_{sn}}$	2.8 $m\Omega$
Capacitor - Capacitance	C_{sn}	660 nF
Capacitor - ESR	$R_{C_{sn}}$	0.5 Ω
Resistor - Resistance	R_{sn}	100 Ω
Output diode		
Forward threshold voltage	$V_{T,D}$	1.35 V
Forward voltage drop	$V_{F,D}$	1.35 V
Forward resistance	$R_{D,D}$	17.6 $m\Omega$
Output capacitor		
Capaticance	C	660 nF
ESR	R_C	0.5 Ω

TABLE II
Parameters of the simulation of the transformer in the flyback converter

Parameters	Values
L_m	45 μH
L_{dp}	11.25 μH
L_{ds}	0.37 μH
R_p	80 $m\Omega$
R_s	2.42 Ω

B. Comparison between simulation and experimental prototype

In order to evaluate the quality of the model and the sizing approach and the efficiency of the two layout of the converter, a use case is selected. The quantities of the source and load of the use case are included in Table III.
The two conversion layouts can supply the same load at same voltage starting from the same source, the main difference is the working point: the FPC works at the maximum duty cycle $D = 0.6$, whereas $D = 0.46$ for the PPC. Fig. 7 and Fig. 8 show the comparison of the voltage in the simulation (light blue lines) and in the experimental prototype (black lines) are shown. Fig. 7 refers to the full power layout, Fig. 8 regards the partial power layout. In the two figures, the plot displays respectively: (a) the source voltage V_{in}, (b) the voltage on the MOSFET, (c) the voltage on the primary side of the transformer, (d) the voltage on the secondary side of the transformer, (e) the voltage of the snubber capacitor, (f) the load voltage V_{out}, (g) the input current of the converter, $i_{in,conv}$, (h) the output current of the converter, $i_{out,conv}$, (i) the output voltage of the converter, $V_{out,conv}$.
The Fig. 7(f) and Fig. 7(i) refer to the same quantity because

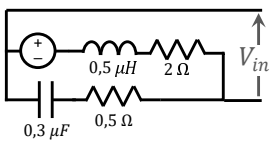

Fig. 6. Basic equivalent electrical model of not ideal voltage generator, used as the source for the simulation of converters.

TABLE III
USE CASE OF THE FLYBACK CONVERTER PROTOTYPE TEST

Parameters	Values
V_{in}	$15V$
V_{out}	$53V$
R_{load}	100Ω

TABLE IV
RESULTS OF THE COMPARISON BETWEEN FPC AND PPC IN TERMS OF POWER AND EFFICIENCY

	FPC	PPC
P_{in}	$53W$	$34.5W$
$P_{in,conv}$	$53W$	$12.3W$
$P_{out,conv}$	$28.8W$	$8.8W$
P_{out}	$28.8W$	$28.7W$
η_{conv}	0.54	0.71
η_{tot}	0.54	0.83
PPF	1	0.31

$v_{out,conv} = v_{out}$ in the only FPC layout. The models and the experimental data in Fig. 7 match well enough. The simulated voltages are not so precise to build a digital double of the converter, but it is useful to verify the limits of the components before testing in various operating conditions. In Fig. 8, the experimental profiles are less close to the simulated ones, this because the input current are affecting the voltage values more than it does in the FPC layout. The inaccurate modeling of the source current is also clear from Fig. 7(g) and Fig. 8(g).
Based on the voltage in Fig. 7(b) and Fig. 8(b) and the current values from Fig. 7(g) and Fig. 8(g), the mosfet in the PPC does not seem to be less stressed than that in the FPC layout. The estimated power losses on the prototype's mosfet are around $1W$ in both layouts. Even applying the definition of component stress factor from (14) in [4], the ratio of the stress factors in the two layout comes down to the ratio of the power losses, so it is similar for the two layouts.
Despite this, the global efficiency is improved as presented in Table IV; the PPF of Table IV is the power processing factor defined as $P_{out,conv}/P_{out}$. The PPP layout increased the total efficiency of the conversion system. This is due to two reasons. Firstly, the power bypassing the converter is not affected by the its losses, secondly the converter increased its own efficiency as the consequence of working in a different operating point.

V. CONCLUSION

The aim of this paper is providing a good comparison between the flyback FPC and PPC. The design approach allowed to realize a converter prototype able to work in the two layouts with the same source and load. The modeling approach gave the chance to have an idea of the range of the electrical quantities before and during the implementation.
The models have been able to approximately predict the behaviour of the current and voltage, the weaker matches result in PPC. The reason of the deviation in the model are attributed to the modeling of the source and the high frequency transformer that are not so accurate.
The experimental results confirmed that the PP flyback IPOS implements a true PPP, reducing the power losses on the converter and improving the overall efficiency of the conversion system.

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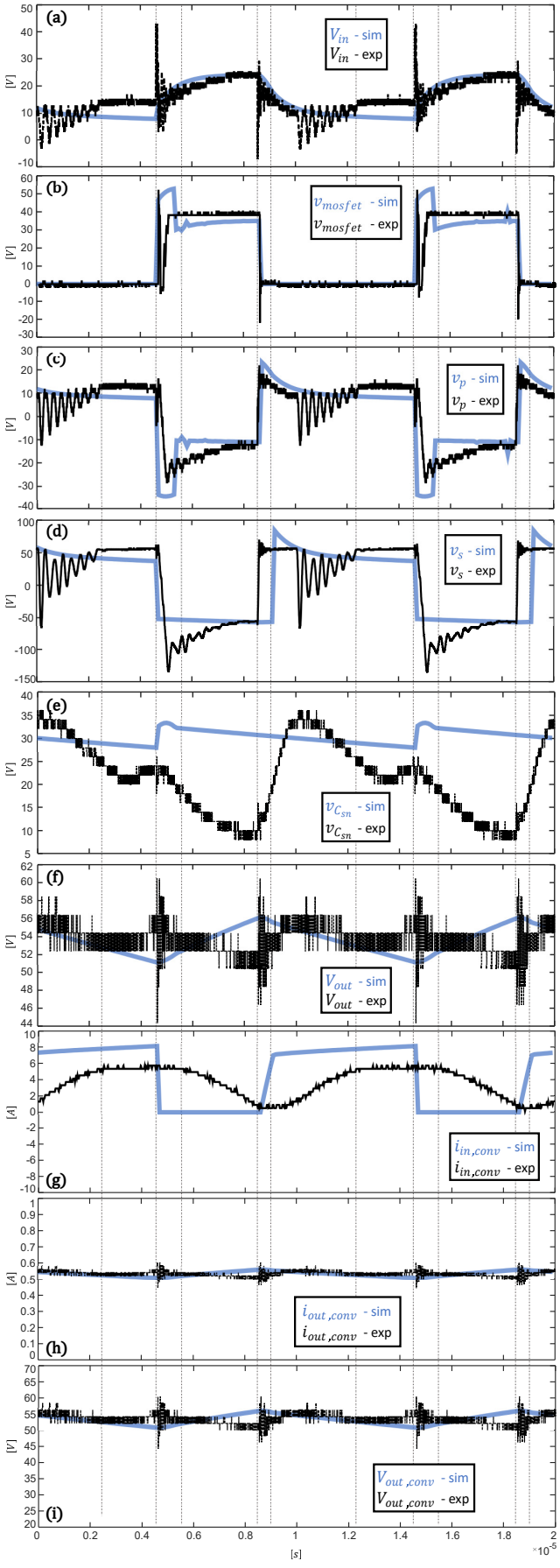

Fig. 7. Comparison of the voltage profiles of the simulation and the experimental results of the full power flyback conversion system.

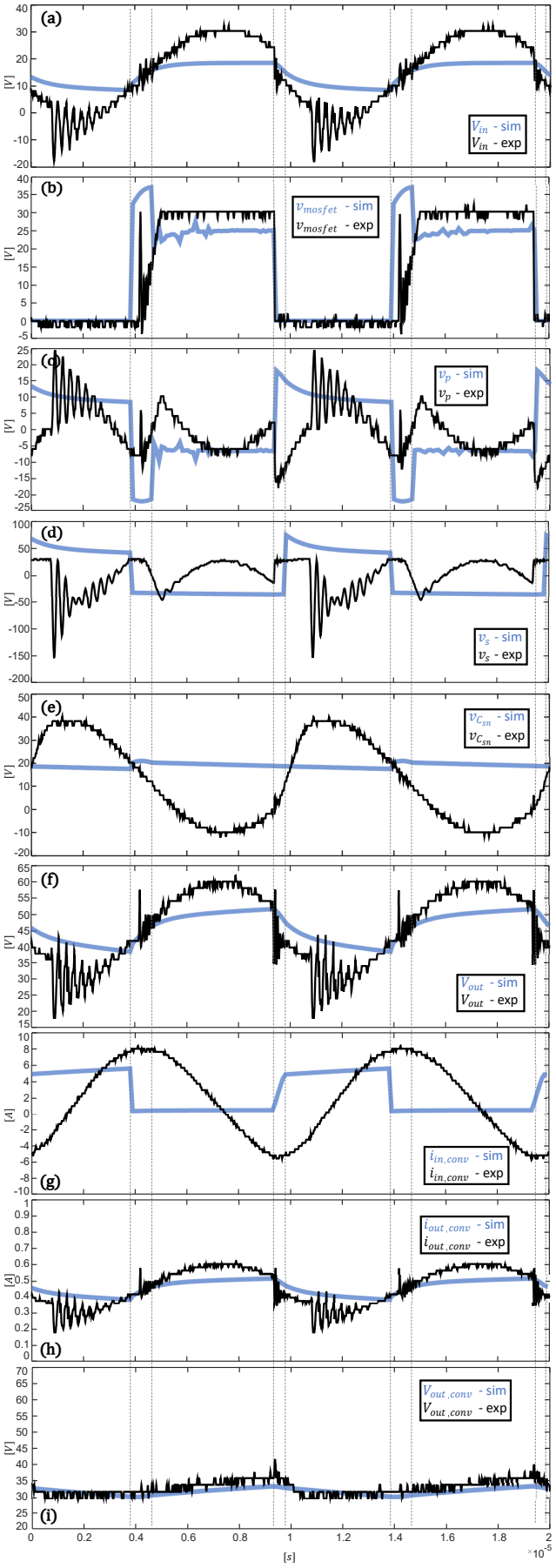

Fig. 8. Comparison of the voltage profiles of the simulation and the experimental results of the partial power flyback conversion system.